

Hardware User Manual

CM-i.MX27 V2.x

...maximum performance at minimum space

Contact

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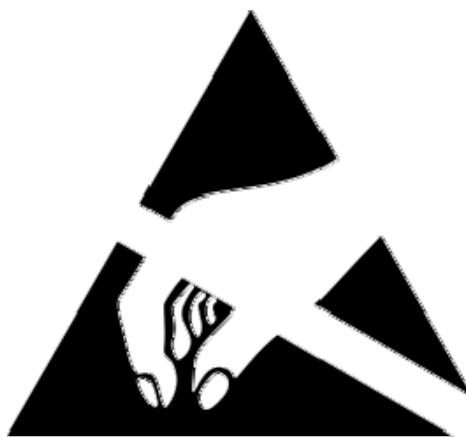
Information

For further information on technology, delivery terms and conditions and prices please contact Bluetechnix (<http://www.bluetechnix.com>).

Warning

Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electro-static charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping



1 Introduction

The CM-i.MX27 is a tiny, high performance and low power ARM9™ based Core Module incorporating Freescale’s high performance i.MX27 Processor. The CM-i.MX27 is available in a Connector version. A BGA version is available on customer request for higher quantities.

The CM-i.MX27 comes with a SMSC Ethernet Transceiver and a SMSC USB-OTG Transceiver. It is both used for development and final application purposes.

The CM-i.MX27 is designed for mobile battery powered applications requiring medium performance.

1.1 Overview

The Core Module CM-i.MX27 consists of the following components. The components are explained in detail below.

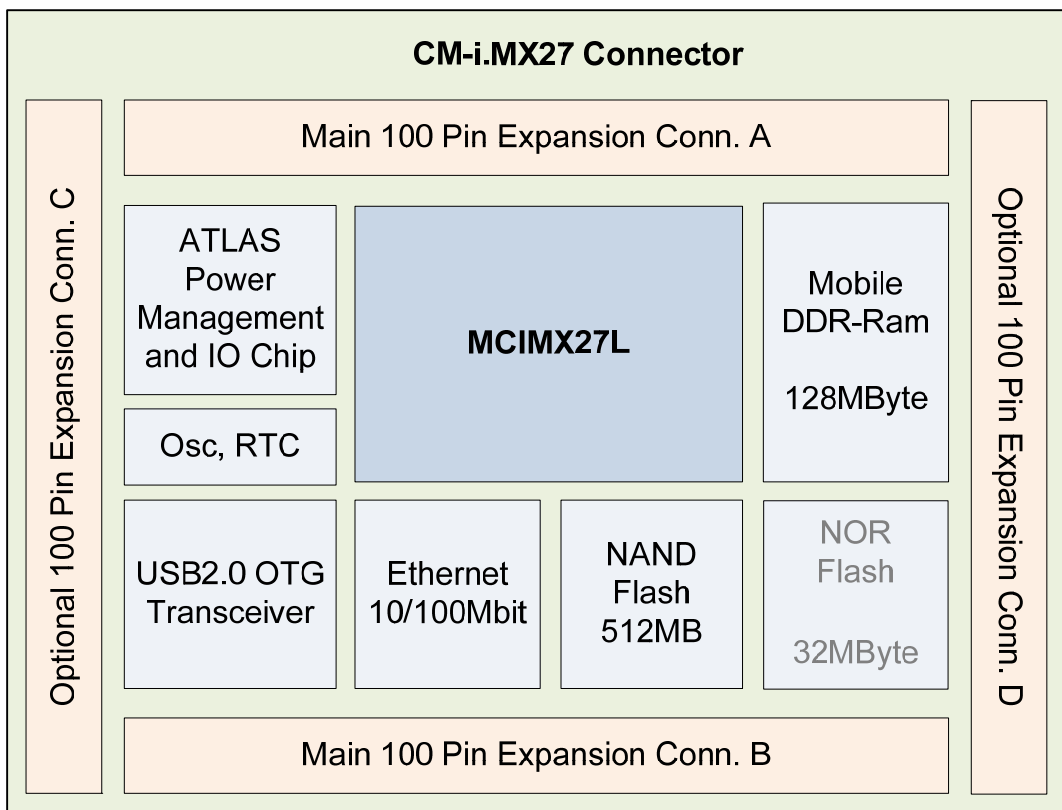


Figure 1-1: Main components of the CM-i.MX27 Core Module

Freescal e.i.MX27L Processor

Functions:

- **Connectivity (internal)**
 - 2x Configurable Serial Peripheral Interface (CSPI)
 - 2x Synchronous Serial Interface (SSI) (I²S and AC97 compliant)
 - 2x Inter IC Connectivity (I²C)
 - Audio Muxer (AUDMUX)

- **Connectivity (external)**
 - 6 x UART
 - USB OTG (High speed)
 - USB Host1 (High speed)
 - USB Host2 (Full speed)
 - 1-Wire interface
 - Fast Ethernet Controller (FEC)

- **Memory Expansion**
 - Secure Digital (SD)
 - Memory Stick Pro
 - SIM
 - ATA

- **External Memory Interface (EMI)**
 - DDR
 - SDRAM
 - NAND Flash
 - PSRAM
 - PC-Card

- **Video Codec and Enhanced Multimedia Accelerator Lite (eMMA_It)**
 - Video Codec
 - Image Preprocessor (PrP)
 - Image Postprocessor (PP)

- **Multimedia Interface**
 - CMOS Sensor Interface (CSI)
 - Smart Liquid Crystal Display Controller (SLCDC)
 - Liquid Crystal Display Controller (LCDC)
 - Keypad Port (KPP)

- **System control**
 - JTAG, ETM
 - Bootstrap
 - System Reset
 - PLL
 - Power Management

- **Core**
 - ARM926EJ-S™ core
 - High Performance ARM® 32-bit engine
 - Smart Speed Switch (MAX)
 - 16Kbytes I-Cache
 - 16Kbytes D-Cache
- **Supported Chips:**
 - i.MX27L
 - i.MX27 (default)

Freescale MC13783 Companion Chip

Energy Management

- Optimized power distribution to increase battery life
 - linear regulators
 - two buck switchers with DVS control
 - One boost switcher
- Ultra low dropout voltage regulator (200mV)
- Switcher frequency adjustment to reduce RF
- Regulators are fully controlled by processors
- Integrated protections (current and temperature)
- Power-up sequencer
- Low-power standby mode
- Integrated multimode charger
 - Trickle, linear, pulse and USB charging modes
 - Accessories supply mode (bottom plug)
 - Charge current controlled by SPI
 - Current and voltage monitored by ADC
 - Overvoltage protections

Audio Interfacing

- Audio Inputs
 - Three amplified inputs and bias for microphone
 - Stereo input for external stereo
- Audio Outputs
 - High-power differential amplifier for earpiece/hands free/polyphonic music
 - Two single-ended amplifiers for stereo headset
 - Earpiece amplifier
- Voice Codec
 - 13-bit linear Tx and Rx mode
 - 8kHz and 16kHz supported
 - Additional ADC for stereo or noise cancellation

- Stereo DAC
 - 16-bit linear/multirate, multiclack modes (PLL)
 - Network mode supported (four slots)
- Audio buses interface
 - Two interchangeable SSI buses
 - Master/slave mode supported

System Control

- On/off phone power cycling
 - On/off state machine
 - Power-up events (on/off switch buttons, alarms)
 - Power-off events (watchdog failure, OV, UV, temperature)
- Reset
 - System RST output
 - MCU RST for warm start
 - Warm/cold start flag
- Specific power modes (for battery life optimization)
 - Memory hold mode
 - User off mode

Analog Sensor Control

- 10-bit ADC
- Four-wire resistive touch-screen interface
- Thermal bias (battery)
- Eight internal sense channels (including voltage and current reading on battery and charger)
- Fully controlled via SPI
- Programmable digital comparators

Peripherals

- Lighting
 - Three backlight drivers for LCDs and keypad
 - Programmable level and PWM control
 - Three sets of RGB tricolor LED drivers
 - Programmable level and PWM control
 - Vibrator interface for signaling

Clocks and timing

- Clocks

- 32kHz system clock
- Two clock outputs with different power bank

- Real-Time-Clock
 - Time and date
 - Alarm including phone wake-up functions
 - Timebase by crystal oscillator
 - System timekeeping
 - Supply backup by coin cell
 - RC mode until crystal is stabilized

Current Consumption

- Standby mode (RTC and regulators into low-power mode): 140 μ A
- Off mode (RTC and core logic): 30 μ A
- RTC only: 5 μ A

Mobile DDR-SDRAM

- 2x MT46H32M16LFCK-6 (512Mbit) (default)

NAND Flash

- MT29F4G08ABCW (default)
- 512M x 8 (4Gbit), 1.8V IO Voltage
- Different NAND Flashes in TSOP48 package available upon request. Micron, Samsung, ST Microelectronics.

Intel Strata Boot Flash

- PF48F4000P0ZBQE
- 32MB Flash: 16M x 16 (256 Mbit)

USB OTG Transceiver

- USB3317
- High Speed USB Transceiver
- 1.8V-3.3V ULPI Transceiver

Physical Ethernet Transceiver

- LAN8700
- 10Base-T / 100Base-TX
- Auto cable crossover detection and correction

1.2 Target Applications

- **Industrial PDA**
- **Medical Devices**
- **Low cost point of sale terminal module**
- **Generic medium performance multimedia processor module**
- **Multimedia Application Processor Module**
- **Internet Connected Embedded System**
- **Portable devices**

2 Specification

2.1 Functional Specification

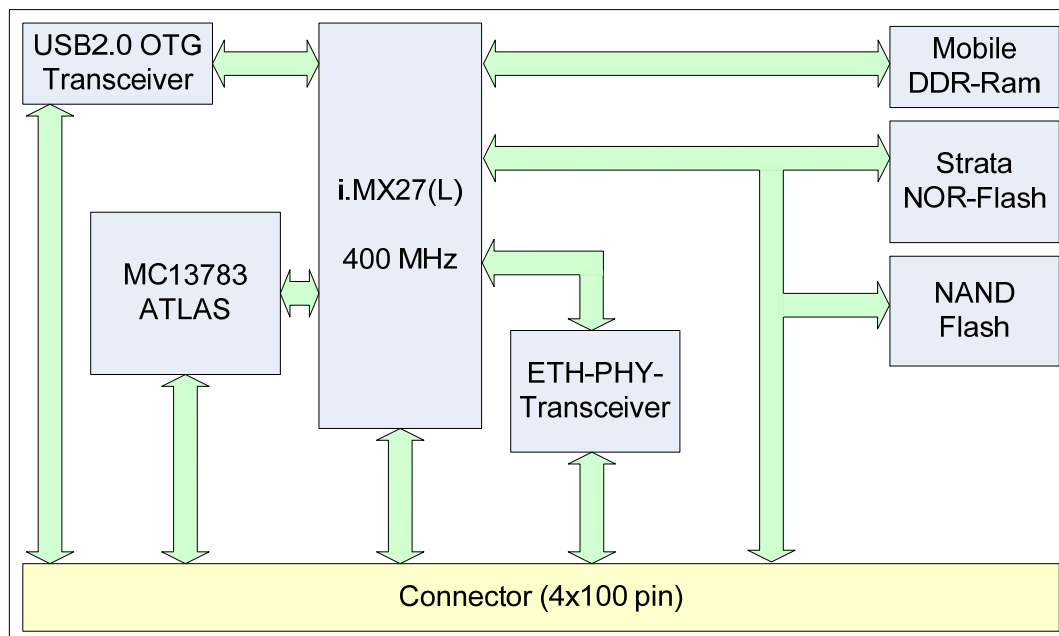


Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the CM-i.MX27 Core Module.

2.2 Boot Mode

The Core Module supports several boot modes. Table 2-1 shows the different boot modes and their boot functions. 0 is the logical low voltage level and a 1 stands for the logical high level. The power bank from the boot mode pins is AVDD (P_VRF2). For special information about the boot modes please refer to the i.MX27 reference manual which is available from Freescale's website. The most common used bootmodes are printed bold.

BOOT3	BOOT2	BOOT1	BOOT0	Function	Boot Address
0	0	0	0	iROM Bootstrap USB/UART	0x0000'0030
0	0	0	1	reserved	2.2.1
0	0	1	0	8-bit NAND Flash (2 Kbytes per page)	0xD800'0000
0	0	1	1	16-bit NAND Flash (2 Kbytes per page)	0xD800'0000
0	1	0	0	16-bit NAND Flash (512 bytes per page)	0xD800'0000
0	1	0	1	16-bit CS0 at D[15:0] (NOR Flash)	0xC800'0000
0	1	1	0	reserved	2.2.2
0	1	1	1	8-bit NAND Flash (512 bytes per page)	0xD800'0000
1	X	X	X	reserved	2.2.3

Table 2-1: Boot Modes

2.3 EMI Memory map

The EMI supports 4 different memory controllers. Table 2-2 illustrates the memory map for the default board configuration.

Memory Type	Start Address	End Address	Maxsize	i.MX CS	Comment
DDR SD-RAM	0xA000'0000	0xAFFF'FFFF	256MB	CSD0/CS2	2x16bit Micron DDR
P30 Strata Flash	0xC000'0000	0xC1FF'FFFF	32MB	CS0	16bit Bus

Table 2-2: Memory Map

2.4 Power Domains

Table 2-3 lists the power domains and their associated power sources. Further, the power up sequence and the default voltage level after a power up are given. Please note that not all Domains can be changed later without affecting the functionality of the Core Module.

Domain on i.MX27	Power	Voltage Level	Power-Up Seq.
QVDD	P_SW1	1.2V	4,5
NVDD1, NVDD2, NVDD3, NVDD4, NVDD6, NVDD7, FUSE_VDD	P_SW2	1.8V	7,8
-	P_SW3_(P_BOOST)	5.5V	1
-	P_VAUDIO	2.775V	11
NVDD14, NVDD15	P_VIOHI	2.775V	6
-	P_VIOLO	1.8V	6
-	P_VDIG	1.2V	9
-	P_VRFDIG	1.875V	6
-	P_VRFREF	2.775V	3
-	P_VRFBG	2.775V	11
-	P_VRFBG	1.2V	11
-	P_VSIM	off	10
-	P_VESIM	off	10
FPMVDD, MPLLVD, UPLLVD	P_VGEN	1.5V	6
NVDD11	P_VCAM	off	9
-	P_VRF1	2.775V	12
VDD5, NVDD9, NVDD12, NVDD13, AVDD, OSC26VDD	P_VRF2	2.775V	13
NVDD8	P_VMMC1	P_VRF2-0.3V	14
NVDD10	P_VMMC2	off	15
-	P_VBKUP1	off	3
-	P_VBKUP2	off	9
-	VUSB	off	2
-	VBUS	off	2

Table 2-3: Power-Domain-Map and Power-Up Sequence

For more information about the power up sequence and default voltage levels see the MC13783 user guide and the MCIMX27 reference manual.

2.5 Internal Reset Routing

Figure 2-2 shows the Reset signal routing on the Core Module.

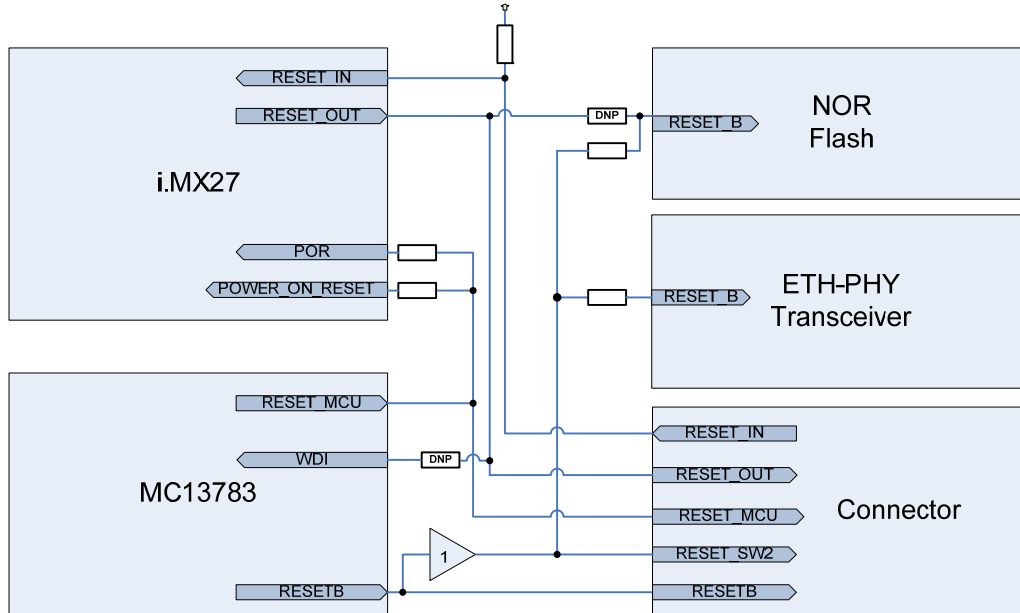


Figure 2-2: Reset Domains with mount options

2.5.1 i.MX Resets

- **RESET_IN_B:** This signal is the main reset input, and can be connected to an external reset-button that shorts the signal to GND. The signal is pulled up on the Core Module to P_VRF2.
- **POWER_ON_RESET:** is directly connected to the MC13783 RESETB_MCU signal.
- **POR_B:** is directly connected to the MC13783 RESETB_MCU signal.
- **RESET_OUT_B:** This signal can be used to reset external devices.

2.5.2 MC13783 Resets

- **RESETB:** This signal can be used to reset external devices, and it is internally pulled up to P_VRF2.
- **RESETB_MCU:** This signal is connected to the POR_B and POWER_ON_B pins of the i.MX27.
- **WDI:** This signal is pulled up to P_ATLAS, and can be connected to the RESET_OUT_B i.MX signal in case the Watchdog functionality is needed (**open by default!**).
- **RESETB_SW2:** This signal is a level-shifted version of the RESETB signal to P_SW2.

2.5.3 Peripheral Resets

- LAN8700 (Ethernet Physical): connected to RESETB_SW2.
- PF48F4000P0ZBQE (Flash): connected to RESETB_SW2 (mount option to RESET_OUT).

2.6 Internal Clock Distribution

Figure 2-3 shows an overview of the internal clock routing on the Core Module. The Interfaces shown in the “Connector” Block are externally available.

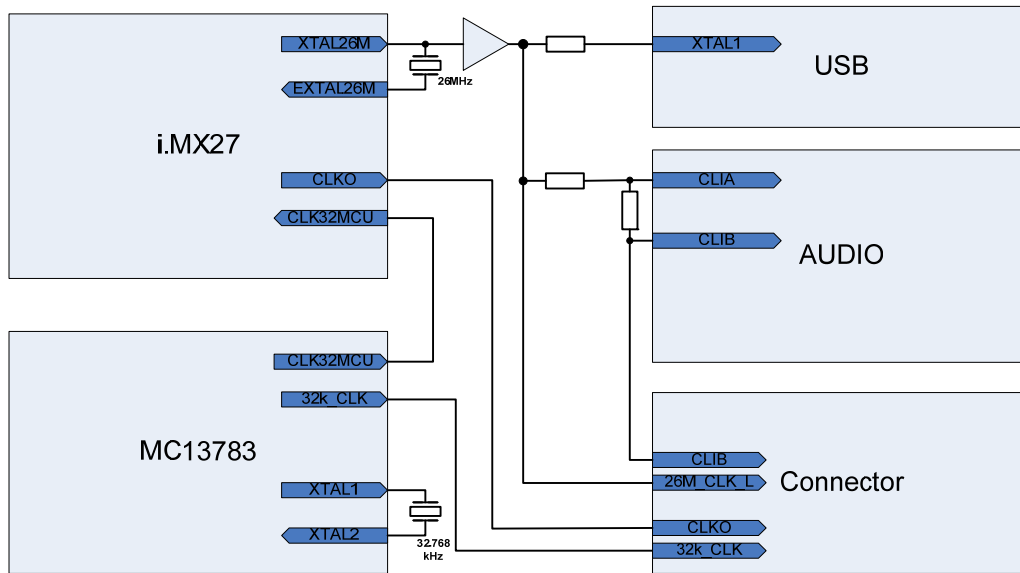


Figure 2-3: Clock Distribution on the Core Module

2.7 Core Module Supply

Figure 2-4 gives an overview, of the power domains on the CM-i.MX27. The battery charger and the voltage regulators are all integrated in the MC13783 Power Management IC. If you need more information about this topic please refer to the MC13783 user guide.

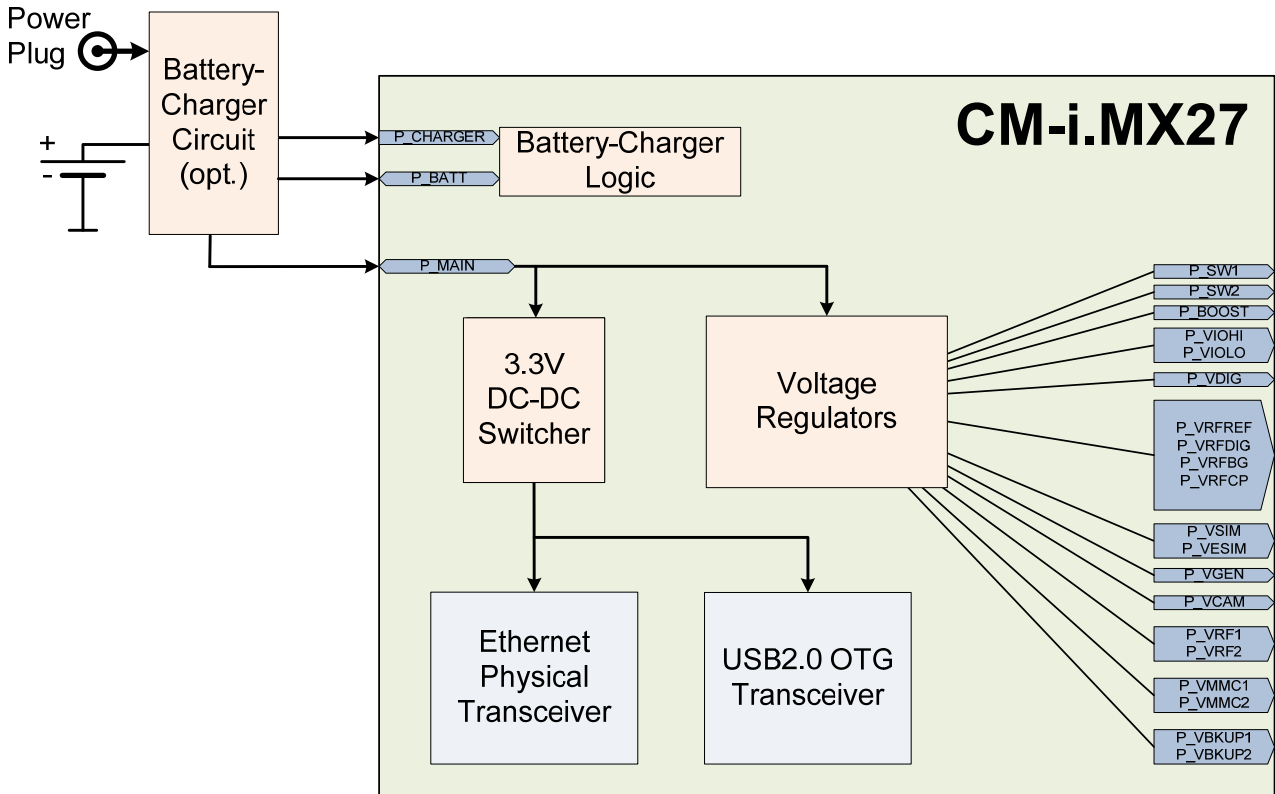


Figure 2-4: Core Module Power

There are two possibilities to power the Core Module. For mobile devices it is recommended to connect a Li-Ion battery to the P_BATT pins to supply the module. When an AC/DC wall adapter is connected to P_CHARGER the battery can be charged. The module works also, if there is no battery connected (or the battery is broken), but the wall adapter is still connected (dead/missing battery mode).

The second way to power the module is to connect the P_MAIN to an external 3.3V stabilized power supply. P_CHARGER must remain unconnected in this case!

2.8 Electrical Specification

2.8.1 Operating Ranges

- **P_MAIN:** 3.3V – 4.65V
- **Li-Ion Battery:** 3.3-4.65V +/-10%
- **Coin cell Voltage (LICELL):** 2.5V to 3.3V
- **P_CHARGER:** 5V to 20V (e.g. AC/DC Wall adapter as charger)

2.8.2 Supply Current

The maximum supply current depends heavily on your application and how the module is powered (P_CHARGER, P_BATT, P_MAIN).

As an average value for power consumption in normal operation (e.g. PDA functionality) 2W can be assumed.

2.9 Environmental Specification

2.9.1 Temperature

- Storage temperature: -40° to 125°C
- Operating temperature: +0°C to + 70°C

2.9.2 Humidity

Operating: 10% to 90% (non condensing)

3 CM-i.MX27C

3.1 Mechanical Outline

All dimensions are given in millimetres!

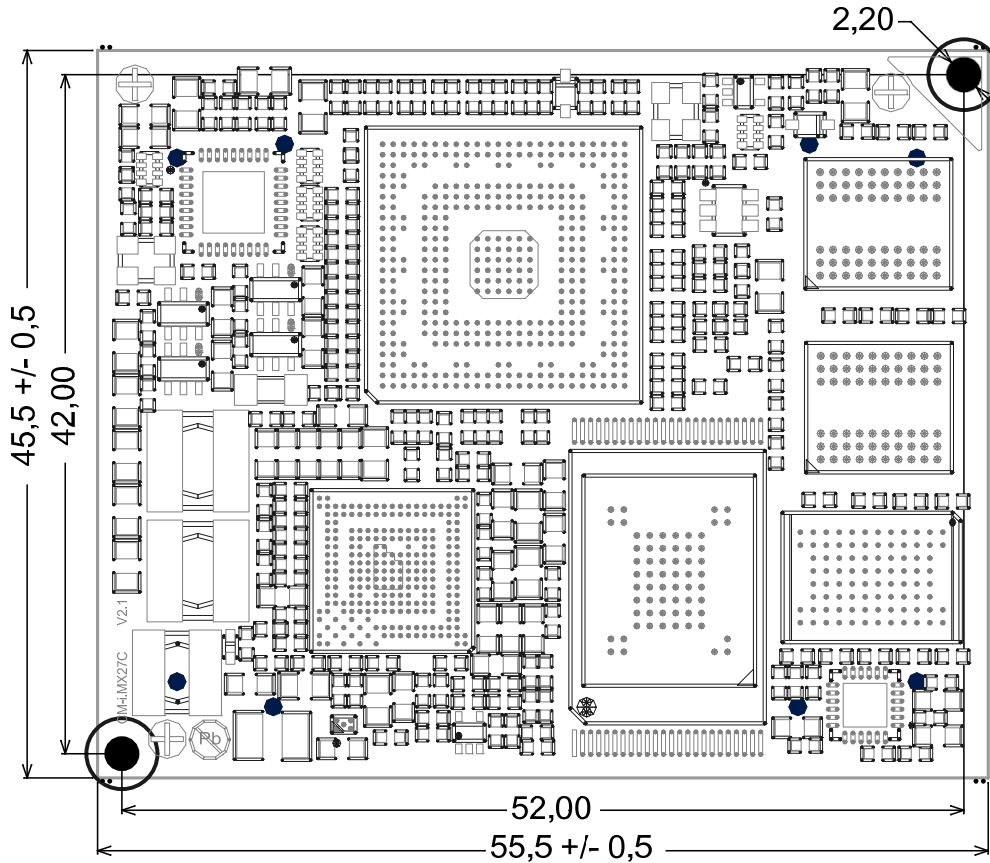


Figure 3-1: Mechanical outline (top view)

The mechanical outline represents a top view; the connectors are placed at the bottom side of the Core Module.

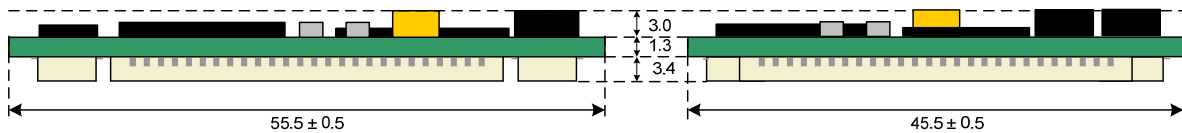


Figure 3-2: Side view with connectors mounted

The total minimum mounting height from the baseboard is 8mm. The stacking height (board to board spacing) is 4mm. It is not recommended to place parts under the Core Module.

3.2 Footprint

For the baseboard the following connectors have to be used.

Part Baseboard	Manufacturer	Manufacturer Part No.
X1 to X4	Hirose	FX10A-100S/10-SV

Table 3-1: Baseboard connector types

The connectors on the CM-i.MX27C are of the following type:

Part	Manufacturer	Manufacturer Part No.
X1 to X4	Hirose 4mm height	FX10A-100P/10-SV

Table 3-2: Core Module connector types

Note: The 5mm height version of the FX10A-100P connector (FX10A-100P/10-SV1) is available upon request!

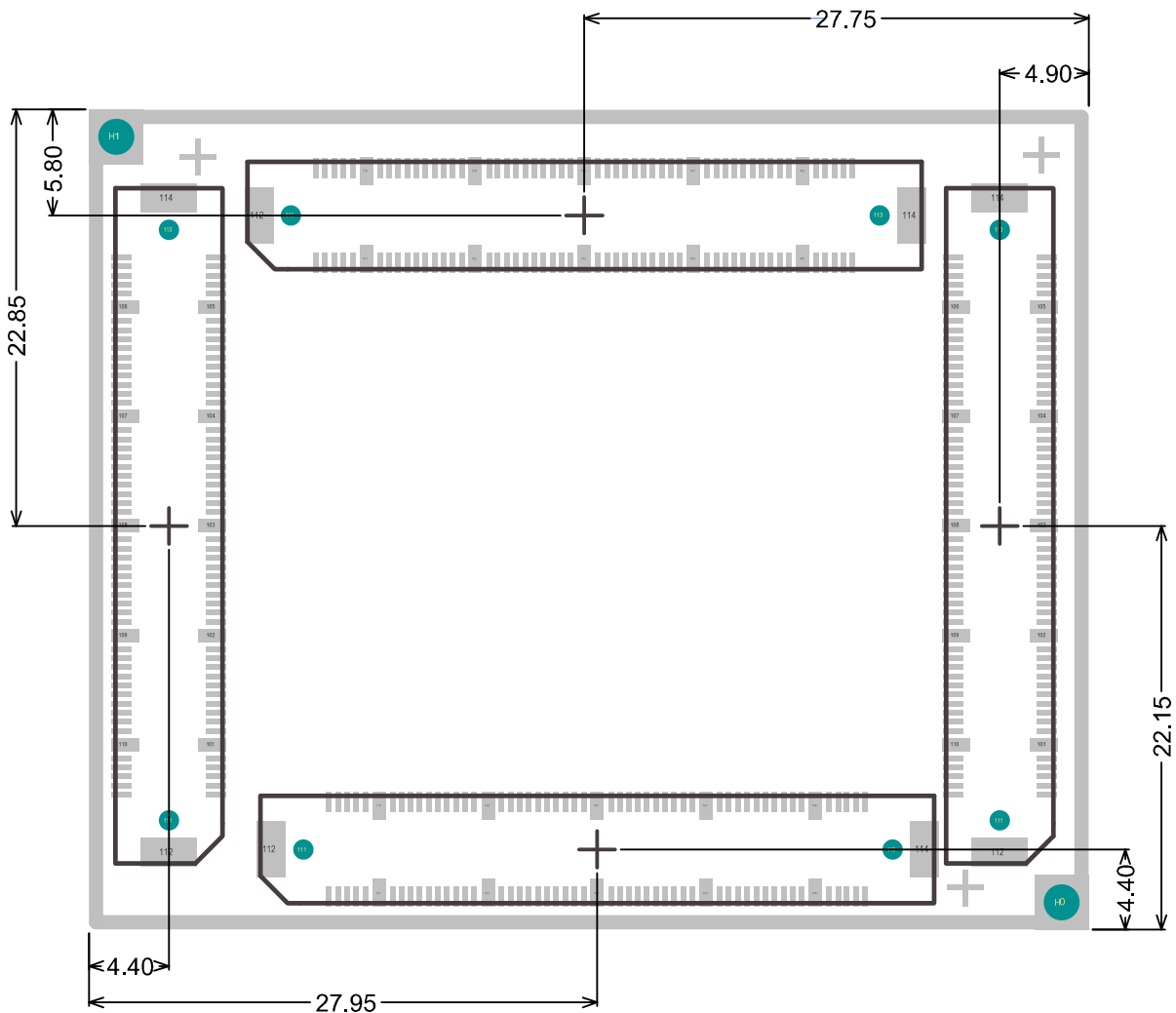


Figure 3-3: FX10A-100P/10-SV connector placement (bottom view)

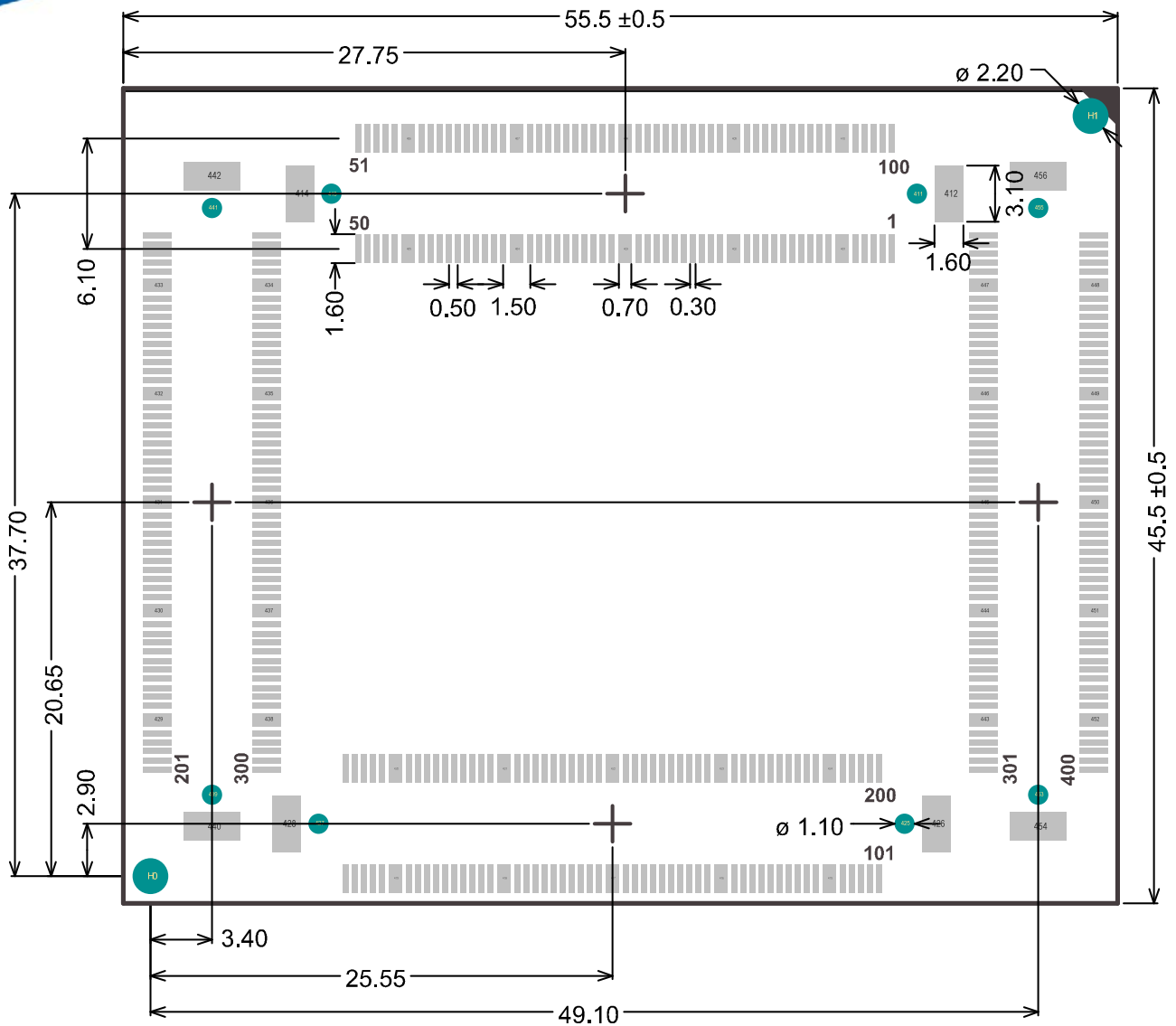


Figure 3-4: Recommended footprint for the Base Board (top view)

For a detailed description of the connector footprints please check the manufacturer's homepage: <http://www.hirose-connectors.com/>.

4 Pin Assignment

4.1 Sub Symbol A – USB

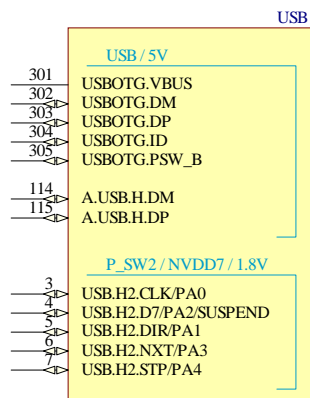


Figure 4-1: Connector Sub-Symbol A - USB

Pin	Name	Group	Type	Power Domain	Device	Description
3	USB.H2.CLK/PA0	NVDD7	I/O	P_SW2	i.MX27	USB Host2 Clock
4	USB.H2.D7/PA2	NVDD7	I/O	P_SW2	i.MX27	USB Host2 Data7
5	USB.H2.DIR/PA1	NVDD7	I/O	P_SW2	i.MX27	USB Host2 Direction
6	USB.H2.NXT/PA3	NVDD7	I/O	P_SW2	i.MX27	USB Host2 NEXT
7	USB.H2.STP/PA4	NVDD7	I/O	P_SW2	i.MX27	USB Host2 Stop signal
114	A.USB.H.DM	AT_USB	I/O	P_ATLAS	MC13783	D- pin of the USB cable
115	A.USB.H.DP	AT_USB	I/O	P_ATLAS	MC13783	D+ pin of the USB cable
301	USBOTG.VBUS	USBOTGPHY	POWER	3V3	USB3317	VBUS pin of the USB cable
302	USBOTG.DM	USBOTGPHY	I/O	3V3	USB3317	D- pin of the USB cable
303	USBOTG.DP	USBOTGPHY	I/O	3V3	USB3317	D+ pin of the USB cable
304	USBOTG.ID	USBOTGPHY	I	3V3	USB3317	ID pin of the USB cable
305	USBOTG.PSW_B	USBOTGPHY	O	3V3	USB3317	External 5 Volt supply enable

Table 4-1: Connector Sub-Symbol A – USB

4.2 Sub Symbol B – IPU

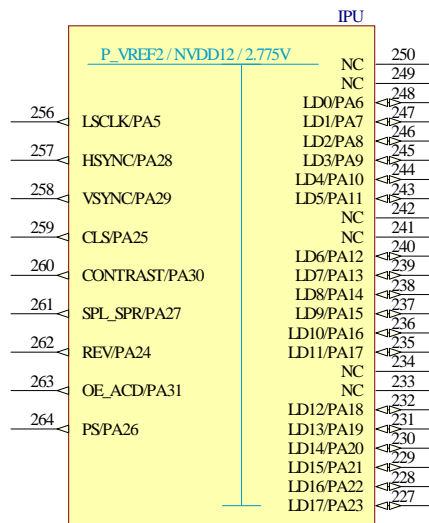


Figure 4-2: Connector Sub-Symbol B - IPU

Pin	Name	Group	Type	Power Domain	Device	Description
227	LD17/PA23	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
228	LD16/PA22	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
229	LD15/PA21	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
230	LD14/PA20	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
231	LD13/PA19	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
232	LD12/PA18	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
233	NC	4.2.1	4.2.2	4.2.3	4.2.4	4.2.5
234	NC	4.2.6	4.2.7	4.2.8	4.2.9	4.2.10
235	LD11/PA17	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
236	LD10/PA16	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
237	LD9/PA15	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
238	LD8/PA14	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
239	LD7/PA13	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
240	LD6/PA12	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
241	NC					

Pin	Name	Group	Type	Power Domain	Device	Description
242	NC	4.2.11	4.2.12	4.2.13	4.2.14	4.2.15
243	LD5/PA11	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
244	LD4/PA10	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
245	LD3/PA9	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
246	LD2/PA8	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
247	LD1/PA7	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
248	LD0/PA6	IPU	I/O	P_VREF2	i.MX27	LCD Data Bus
249	NC	4.2.16	4.2.17	4.2.18	4.2.19	4.2.20
250	NC	4.2.21	4.2.22	4.2.23	4.2.24	4.2.25
256	LSCLK/PA5	IPU	O	P_VREF2	i.MX27	Shift Clock
257	HSYNC/PA28	IPU	O	P_VREF2	i.MX27	Line Pulse or HSync
258	VSYNC/PA29	IPU	O	P_VREF2	i.MX27	Frame Sync or Vsync - This signal also serves as the clock signal output for gate
259	CLS/PA25	IPU	O	P_VREF2	i.MX27	Start signal output for gate driver
260	CONTRAST/PA30	IPU	O	P_VREF2	i.MX27	This signal is used to control the LCD bias voltage as contrast control
261	SPL_SPR/PA27	IPU	O	P_VREF2	i.MX27	Sampling start signal for left and right scanning
262	REV/PA24	IPU	O	P_VREF2	i.MX27	Signal for common electrode driving signal preparation
263	OE_ACD/PA31	IPU	O	P_VREF2	i.MX27	Alternate Crystal Direction/Output Enable
264	PS/PA26	IPU	O	P_VREF2	i.MX27	Control signal output for source driver

Table 4-2: Connector Sub-Symbol B – IPU

4.3 Sub Symbol C – UART

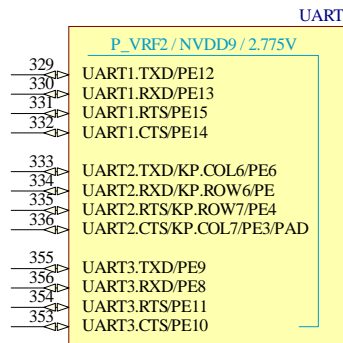


Figure 4-3: Connector Sub-Symbol C - UART

Pin	Name	Group	Type	Power Domain	Device	Description
329	UART1.TXD/PE12	UART	O	P_VRF2	i.MX27	Transmit Data
330	UART1.RXD/PE13	UART	I	P_VRF2	i.MX27	Receive Data
331	UART1.RTS/PE15	UART	I	P_VRF2	i.MX27	Request to Send
332	UART1.CTS/PE14	UART	O	P_VRF2	i.MX27	Clear to Send
333	UART2.TXD/KP.COL6/PE6	UART	O	P_VRF2	i.MX27	Transmit Data
334	UART2.RXD/KP.ROW6/PE5	UART	I	P_VRF2	i.MX27	Receive Data
335	UART2.RTS/KP.ROW7/PE4	UART	I	P_VRF2	i.MX27	Request to Send
336	UART2.CTS/KP.COL7/PE3	UART	O	P_VRF2	i.MX27	Clear to Send
355	UART3.TXD/PE9	UART	O	P_VRF2	i.MX27	Transmit Data
356	UART3.RXD/PE8	UART	I	P_VRF2	i.MX27	Receive Data
357	UART3.RTS/PE11	UART	I	P_VRF2	i.MX27	Request to Send
358	UART3.CTS/PE10	UART	O	P_VRF2	i.MX27	Clear to Send

Table 4-3: Connector Sub-Symbol C - UART

4.4 Sub Symbol D – SD/I2C/SSI

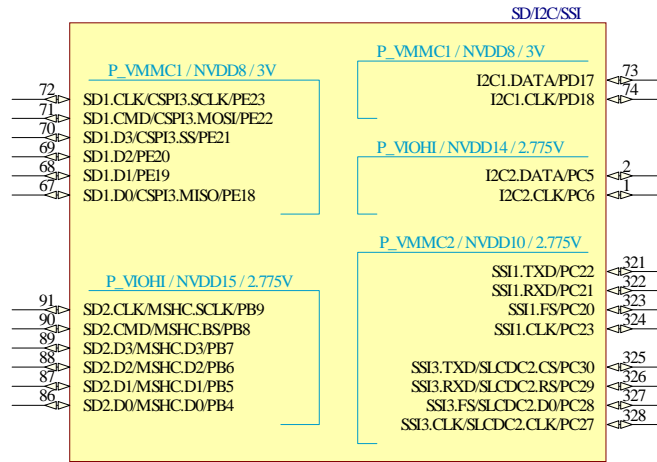


Figure 4-4: Connector Sub-Symbol D – SD/I2C/SSI

Pin	Name	Group	Type	Power Domain	Device	Description
1	I2C2.CLK/PC6	I2C	I/O	P_VIOHI	i.MX27	I2C2 Clock
1	I2C2.DATA/PC5	I2C	I/O	P_VIOHI	i.MX27	I2C2 Data
67	SD1.D0/CSPI3.MISO/PE18	SD	I/O	P_VMMC1	i.MX27	SD Data
68	SD1.D1/PE19	SD	I/O	P_VMMC1	i.MX27	SD Data
69	SD1.D2/PE20	SD	I/O	P_VMMC1	i.MX27	SD Data
70	SD1.D3/CSPI3.SS/PE21	SD	I/O	P_VMMC1	i.MX27	SD Data
71	SD1.CMD/CSPI3.MOSI/PE22	SD	I/O	P_VMMC1	i.MX27	SD Command
72	SD1.CLK/CSPI3.SCLK/PE23	SD	I/O	P_VMMC1	i.MX27	SD Output Clock
73	I2C1.DATA/PD17	I2C	I/O	P_VMMC1	i.MX27	I2C1 Data
74	I2C1.CLK/PD18	I2C	I/O	P_VMMC1	i.MX27	I2C1 Clock
86	SD2.D0/MSHC.D0/PB4	SD	I/O	P_VIOHI	i.MX27	SD Data
87	SD2.D1/MSHC.D1/PB5	SD	I/O	P_VIOHI	i.MX27	SD Data
88	SD2.D2/MSHC.D2/PB6	SD	I/O	P_VIOHI	i.MX27	SD Data
89	SD2.D3/MSHC.D3/PB7	SD	I/O	P_VIOHI	i.MX27	SD Data
90	SD2.CMD/MSHC.BS/PB8	SD	I/O	P_VIOHI	i.MX27	SD Command
91	SD2.CLK/MSHC.SCLK/PB9	SD	I/O	P_VIOHI	i.MX27	SD Output Clock

Pin	Name	Group	Type	Power Domain	Device	Description
321	SSI1.TXD/PC22	SSI	I/O	P_VMMC2	i.MX27	Transmit serial data
322	SSI1.RXD/PC21	SSI	I/O	P_VMMC2	i.MX27	Receive serial data
323	SSI1.FS/PC20	SSI	I/O	P_VMMC2	i.MX27	Frame Sync signal
324	SSI1.CLK/PC23	SSI	I/O	P_VMMC2	i.MX27	Serial clock signal
325	SSI3.TXD/SLCDC2.CS/PC30	SSI	I/O	P_VMMC2	i.MX27	Transmit serial data
326	SSI3.RXD/SLCDC2.RS/PC29	SSI	I/O	P_VMMC2	i.MX27	Receive serial data
327	SSI3.FS/SLCDC2.D0/PC28	SSI	I/O	P_VMMC2	i.MX27	Frame Sync signal
328	SSI3.CLK/SLCDC2.CLK/PC27	SSI	I/O	P_VMMC2	i.MX27	Serial clock signal

Table 4-4: Connector Sub-Symbol D – SD/I2C/SSI

4.5 Sub Symbol E – CSI

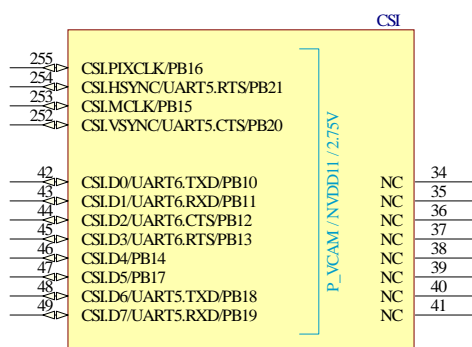


Figure 4-5: Connector Sub-Symbol C - CSI

Pin	Name	Group	Type	Power Domain	Device	Description
34	NC					4.5.1
35	NC	4.5.2	4.5.3	4.5.4	4.5.5	
36	NC					4.5.6
37	NC	4.5.7	4.5.8	4.5.9	4.5.10	
38	NC					4.5.11
39	NC	4.5.12	4.5.13	4.5.14	4.5.15	
40	NC					4.5.16
41	NC	4.5.17	4.5.18	4.5.19	4.5.20	
42	CSI.D0/UART6.TXD/PB10	CSI	I/O	P_VCAM	i.MX27	Sensor port data
43	CSI.D1/UART6.RXD/PB11	CSI	I/O	P_VCAM	i.MX27	Sensor port data
44	CSI.D2/UART6.CTS/PB12	CSI	I/O	P_VCAM	i.MX27	Sensor port data
45	CSI.D3/UART6.RTS/PB13	CSI	I/O	P_VCAM	i.MX27	Sensor port data
46	CSI.D4/PB14	CSI	I/O	P_VCAM	i.MX27	Sensor port data
47	CSI.D5/PB17	CSI	I/O	P_VCAM	i.MX27	Sensor port data
48	CSI.D6/UART5.TXD/PB18	CSI	I/O	P_VCAM	i.MX27	Sensor port data
49	CSI.D7/UART5.RXD/PB19	CSI	I/O	P_VCAM	i.MX27	Sensor port data
252	CSI.VSYNC/UART5.CTS/PB20	CSI	I/O	P_VCAM	i.MX27	Sensor port vertical sync,
253	CSI.MCLK/PB15	CSI	I/O	P_VCAM	i.MX27	Sensor port master clock

Pin	Name	Group	Type	Power Domain	Device	Description
254	CSI.HSYNC/UART5.RTS/PB21	CSI	I/O	P_VCAM	i.MX27	Sensor port horizontal sync
255	CSI.PIXCLK/PB16	CSI	I/O	P_VCAM	i.MX27	Sensor port data latch clock

Table 4-5: Connector Sub-Symbol E – CSI

4.6 Sub Symbol F - EMI

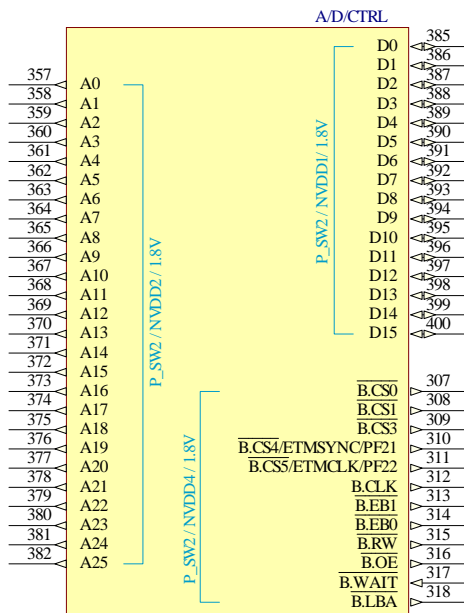


Figure 4-6: Connector Sub-Symbol F - EMI

Pin	Name	Group	Type	Power Domain	Device	Description
307	nB.CS0	EMI	Output	P_SW2	i.MX27	Chip Select
308	nB.CS1	EMI	Output	P_SW2	i.MX27	Chip Select
309	nB.CS3	EMI	Output	P_SW2	i.MX27	Chip Select
310	nB.CS4/ETMSYNC/PF21	EMI	Output	P_SW2	i.MX27	Chip Select
311	n.BCS5/ETMCLK/PF22	EMI	Output	P_SW2	i.MX27	Chip Select
312	B.CLK	EMI	Output	P_SW2	i.MX27	Clock signal sent to external synchronous memories during burst mode
313	nB.EB1	EMI	Output	P_SW2	i.MX27	Active low external enable byte signal that controls D [7:0]
314	nB.EB0	EMI	Output	P_SW2	i.MX27	Active low external enable byte signal that controls D [15:8]
315	nB.RW	EMI	Output	P_SW2	i.MX27	RW signal
316	nB.OE	EMI	Output	P_SW2	i.MX27	Memory Output Enable

Pin	Name	Group	Type	Power Domain	Device	Description
317	nB.WAIT	EMI	Input	P_SW2	i.MX27	Active low input signal sent by flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence
318	nB.LBA	EMI	Output	P_SW2	i.MX27	Active low signal sent by flash device causing external burst device to latch the starting burst address
357	A0	EMI	Output	P_SW2	i.MX27	Address bus signal
358	A1	EMI	Output	P_SW2	i.MX27	Address bus signal
359	A2	EMI	Output	P_SW2	i.MX27	Address bus signal
360	A3	EMI	Output	P_SW2	i.MX27	Address bus signal
361	A4	EMI	Output	P_SW2	i.MX27	Address bus signal
362	A5	EMI	Output	P_SW2	i.MX27	Address bus signal
363	A6	EMI	Output	P_SW2	i.MX27	Address bus signal
364	A7	EMI	Output	P_SW2	i.MX27	Address bus signal
365	A8	EMI	Output	P_SW2	i.MX27	Address bus signal
366	A9	EMI	Output	P_SW2	i.MX27	Address bus signal
367	A10	EMI	Output	P_SW2	i.MX27	Address bus signal
368	A11	EMI	Output	P_SW2	i.MX27	Address bus signal
369	A12	EMI	Output	P_SW2	i.MX27	Address bus signal
370	A13	EMI	Output	P_SW2	i.MX27	Address bus signal
371	A14	EMI	Output	P_SW2	i.MX27	Address bus signal
372	A15	EMI	Output	P_SW2	i.MX27	Address bus signal
373	A16	EMI	Output	P_SW2	i.MX27	Address bus signal
374	A17	EMI	Output	P_SW2	i.MX27	Address bus signal
375	A18	EMI	Output	P_SW2	i.MX27	Address bus signal

Pin	Name	Group	Type	Power Domain	Device	Description
376	A19	EMI	Output	P_SW2	i.MX27	Address bus signal
377	A20	EMI	Output	P_SW2	i.MX27	Address bus signal
378	A21	EMI	Output	P_SW2	i.MX27	Address bus signal
379	A22	EMI	Output	P_SW2	i.MX27	Address bus signal
380	A23	EMI	Output	P_SW2	i.MX27	Address bus signal
381	A24	EMI	Output	P_SW2	i.MX27	Address bus signal
382	A25	EMI	Output	P_SW2	i.MX27	Address bus signal
385	D0	EMI	I/O	P_SW2	i.MX27	Data Bus signal
386	D1	EMI	I/O	P_SW2	i.MX27	Data Bus signal
387	D2	EMI	I/O	P_SW2	i.MX27	Data Bus signal
388	D3	EMI	I/O	P_SW2	i.MX27	Data Bus signal
389	D4	EMI	I/O	P_SW2	i.MX27	Data Bus signal
390	D5	EMI	I/O	P_SW2	i.MX27	Data Bus signal
391	D6	EMI	I/O	P_SW2	i.MX27	Data Bus signal
392	D7	EMI	I/O	P_SW2	i.MX27	Data Bus signal
393	D8	EMI	I/O	P_SW2	i.MX27	Data Bus signal
394	D9	EMI	I/O	P_SW2	i.MX27	Data Bus signal
395	D10	EMI	I/O	P_SW2	i.MX27	Data Bus signal
396	D11	EMI	I/O	P_SW2	i.MX27	Data Bus signal
397	D12	EMI	I/O	P_SW2	i.MX27	Data Bus signal
398	D13	EMI	I/O	P_SW2	i.MX27	Data Bus signal
399	D14	EMI	I/O	P_SW2	i.MX27	Data Bus signal
400	D15	EMI	I/O	P_SW2	i.MX27	Data Bus signal

Table 4-6: Connector Sub-Symbol F - EMI

4.7 Sub Symbol G - KEYPAD

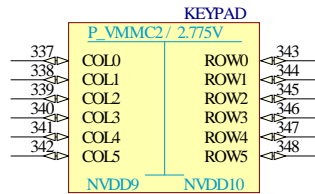


Figure 4-7: Connector Sub-Symbol G - KEYPAD

Pin	Name	Group	Type	Power Domain	Device	Description
337	COL0	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
338	COL1	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
339	COL2	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
340	COL3	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
341	COL4	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
342	COL5	Keypad	I/O	P_VRF2	i.MX27	Keypad Column selection signals
343	ROW0	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals
344	ROW1	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals
345	ROW2	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals
346	ROW3	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals
347	ROW4	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals
348	ROW5	Keypad	I/O	P_VRF2	i.MX27	Keypad Row selection signals

Table 4-7: Connector Sub-Symbol G - KEYPAD

4.8 Sub Symbol H - ADIO

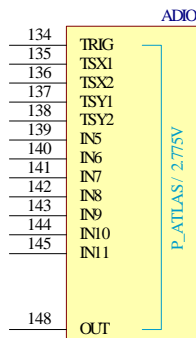


Figure 4-8: Connector Sub-Symbol H - ADIO

Pin	Name	Group	Type	Power Domain	Device	Description
134	TRIG	ADIO	Passive	P_ATLAS	MC13783	ADC trigger input
135	TSX1	ADIO	Passive	P_ATLAS	MC13783	touchscreen input X1 or ADC generic input channel 12
136	TSX2	ADIO	Passive	P_ATLAS	MC13783	touchscreen input X2 or ADC generic input channel 13
137	TSY1	ADIO	Passive	P_ATLAS	MC13783	touchscreen input Y1 or ADC generic input channel 14
138	TSY2	ADIO	Passive	P_ATLAS	MC13783	touchscreen input Y2 or ADC generic input channel 15
139	IN5	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 5
140	IN6	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 6
141	IN7	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 7
142	IN8	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 8
143	IN9	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 9
144	IN10	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 10
145	IN11	ADIO	Passive	P_ATLAS	MC13783	ADC generic input channel 11
148	OUT	ADIO	Passive	P_ATLAS	MC13783	ADC trigger output

Table 4-8: Connector Sub-Symbol H - ADIO

4.9 Sub Symbol I - LED

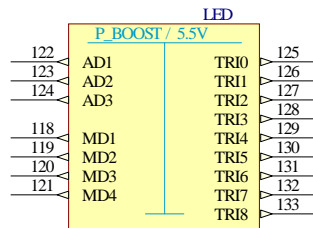


Figure 4-9: Connector Sub-Symbol I - LED

Pin	Name	Group	Type	Power Domain	Device	Description
118	MD1	LED-Driver	Output	P_BOOST	MC13783	Main display backlight LED driver output

Pin	Name	Group	Type	Power Domain	Device	Description
119	MD2	LED-Driver	Output	P_BOOST	MC13783	Main display backlight LED driver output
120	MD3	LED-Driver	Output	P_BOOST	MC13783	Main display backlight LED driver output
121	MD4	LED-Driver	Output	P_BOOST	MC13783	Main display backlight LED driver output
122	AD1	LED-Driver	Output	P_BOOST	MC13783	Auxiliary display backlight LED driver output
123	AD2	LED-Driver	Output	P_BOOST	MC13783	Auxiliary display backlight LED driver output
124	AD3	LED-Driver	Output	P_BOOST	MC13783	Keypad lighting LED driver output
125	TRI0	LED-Driver	Output	P_BOOST	MC13783	Tricolor green LED driver output
126	TRI1	LED-Driver	Output	P_BOOST	MC13783	Tricolor red LED driver output
127	TRI2	LED-Driver	Output	P_BOOST	MC13783	Tricolor blue LED driver output
128	TRI3	LED-Driver	Output	P_BOOST	MC13783	Tricolor green LED driver output
129	TRI4	LED-Driver	Output	P_BOOST	MC13783	Tricolor red LED driver output
130	TRI5	LED-Driver	Output	P_BOOST	MC13783	Tricolor blue LED driver output
131	TRI6	LED-Driver	Output	P_BOOST	MC13783	Tricolor green LED driver output
132	TRI7	LED-Driver	Output	P_BOOST	MC13783	Tricolor red LED driver output
133	TRI8	LED-Driver	Output	P_BOOST	MC13783	Tricolor blue LED driver output

Table 4-9: Connector Sub-Symbol I - LED

4.10 Sub Symbol J – POWER-OUT

POWER_OUT			
101	P_SW1	P_BOOST	116
383	P_SW1	P_BOOST	117
384	P_SW1		
8	P_SW2	P_ATLAS	202
9	P_SW2		
10	P_SW2	P_AUDIO	195
110	NC		
111	NC	P_VRF1	217
112	NC	P_VRF2	219
113	NC	P_VRF3	221
		P_VRF4	223
276	P_VRF1	GND	85
277	P_VRF1	GND	93
33	P_VRF2	GND	109
265	P_VRF2	GND	150
		GND	196
		GND	197
75	P_VMMC1	GND	199
76	P_VMMC1	GND	201
349	P_VMMC2	GND	218
350	P_VMMC2	GND	220
		GND	222
274	P_VIOLO	GND	225
92	P_VIOHI	GND	226
		GND	251
224	P_VBKUP1	GND	266
149	P_VBKUP2	GND	267
		GND	268
278	P_VVIB	GND	269
		GND	271
272	P_VDIG	GND	273
		GND	275
270	P_VGEN	GND	300
		GND	306
50	P_VCAM	GND	319
		GND	320
200	P_VSIM	GND	351
198	P_VESIM	GND	352

Figure 4-10: Connector Sub-Symbol J – POWER-OUT

Pin	Name	Group	Type	Power Domain	Device	Description
8, 9, 10	P_SW2	Power	Power	ATLAS	MC13783	I_load_max: 170mA
33, 265	P_VRF2	Power	Power	ATLAS	MC13783	I_load_max: 50mA
50	P_VCAM	Power	Power	ATLAS	MC13783	I_load_max: 90mA
75, 76	P_VMMC1	Power	Power	ATLAS	MC13783	I_load_max: 290mA
92	P_VIOHI	Power	Power	ATLAS	MC13783	I_load_max: 80mA
101, 383, 384	P_SW1	Power	Power	ATLAS	MC13783	I_load_max: 600mA
116, 117	P_BOOST	Power	Power	ATLAS	MC13783	I_load_max: 300mA
149	P_VBKUP2	Power	Power	ATLAS	MC13783	
195	P_AUDIO	Power	Power	ATLAS	MC13783	I_load_max: 200mA
198	P_VESIM	Power	Power	ATLAS	MC13783	I_load_max: 60mA

Pin	Name	Group	Type	Power Domain	Device	Description
200	P_VSIM	Power	Power	ATLAS	MC13783	I_load_max: 60mA
202	P_ATLAS	Power	Power	ATLAS	MC13783	Regulated supply output for the MC13783 core circuitry
217	P_VRFCP	Power	Power	ATLAS	MC13783	I_load_max: 50mA
219	P_VRFREF	Power	Power	ATLAS	MC13783	I_load_max: 50mA
221	P_VRFDIG	Power	Power	ATLAS	MC13783	I_load_max: 200mA
223	P_VRFBG	Power	Power	ATLAS	MC13783	I_load_max: 0,1mA
224	P_VBKUP1	Power	Power	ATLAS	MC13783	4.10.1
270	P_VGEN	Power	Power	ATLAS	MC13783	I_load_max: 140mA
272	P_VDIG	Power	Power	ATLAS	MC13783	I_load_max: 150mA
274	P_VIOLO	Power	Power	ATLAS	MC13783	I_load_max: 150mA
276, 277	P_VRF1	Power	Power	ATLAS	MC13783	I_load_max: 30mA
278	P_VVIB	Power	Power	ATLAS	MC13783	I_load_max: 200mA
349	P_VMMC2	Power	Power	ATLAS	MC13783	I_load_max: 290mA
85, 93, 109, 150, 196, 197, 199, 201, 218, 220, 222, 225, 226, 251, 266, 267, 268, 269, 271, 273, 275, 300, 306, 319, 320, 351, 352	GND	Power	Power	ATLAS	MC13783	Ground
110, 111, 112, 113	NC					

Table 4-10: Connector Sub-Symbol J – POWER-OUT

4.11 Sub Symbol K - CSPI

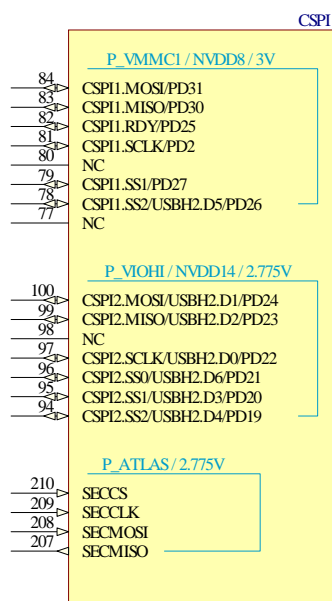


Figure 4-11: Connector Sub-Symbol K - CSPI

Pin	Name	Group	Type	Power Domain	Device	Description
77	NC					4.11.1
78	CSP11.SS2/USBH2.D5/PD26	CSPI	I/O	P_VMMC1	i.MX27	Slave (Selectable signal) Select polarity)
79	CSP11.SS1/PD27	CSPI	I/O	P_VMMC1	i.MX27	Slave (Selectable signal) Select polarity)
80	NC	4.11.2	4.11.3	4.11.4	4.11.5	4.11.6
81	CSP11.SCLK/PD2	CSPI	I/O	P_VMMC1	i.MX27	Serial Clock signal
82	CSP11.RDY/PD25	CSPI	I/O	P_VMMC1	i.MX27	Serial Data Ready signal
83	CSP11.MISO/PD30	CSPI	I/O	P_VMMC1	i.MX27	Master In/Slave Out signal
84	CSP11.MOSI/PD31	CSPI	I/O	P_VMMC1	i.MX27	Master Out/Slave In signal
94	CSP12.SS2/USBH2.D4/PD19	CSPI	I/O	P_VIOHI	i.MX27	Slave (Selectable signal) Select polarity)
95	CSP12.SS1/USBH2.D3/PD20	CSPI	I/O	P_VIOHI	i.MX27	Slave (Selectable signal) Select polarity)

Pin	Name	Group	Type	Power Domain	Device	Description
						signal
96	CSPI2.SS0/USBH2.D6/PD21	CSPI	I/O	P_VIOHI	i.MX27	Slave (Selectable signal) Select polarity
97	CSPI2.SCLK/USBH2.D0/PD22	CSPI	I/O	P_VIOHI	i.MX27	Serial Clock signal
98	NC					4.11.7
99	CSPI2.MISO/USBH2.D2/PD23	CSPI	I/O	P_VIOHI	i.MX27	Master In/Slave Out signal
100	CSPI2.MOSI/USBH2.D1/PD24	CSPI	I/O	P_VIOHI	i.MX27	Master Out/Slave In signal
207	SECMISO	CSPI	Output	P_ATLAS	MC13783	Master In/Slave Out signal
208	SECMOSI	CSPI	Input	P_ATLAS	MC13783	Master Out/Slave In signal
209	SECCLK	CSPI	Input	P_ATLAS	MC13783	Serial Clock signal
210	SECCS	CSPI	Input	P_ATLAS	MC13783	Slave (Selectable signal) Select polarity

Table 4-11: Connector Sub-Symbol K - CSPI

4.12 Sub Symbol L - AUDIO

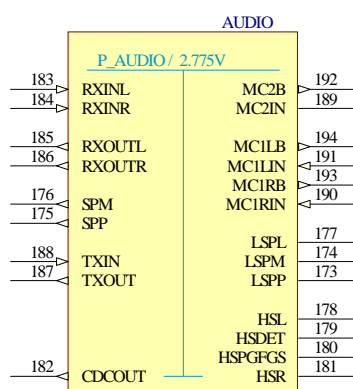


Figure 4-12: Connector Sub-Symbol L - AUDIO

Pin	Name	Group	Type	Power Domain	Device	Description
173	LSP	AUDIO	Passive	P_AUDIO	MC13783	Handset loudspeaker and alert

Pin	Name	Group	Type	Power Domain	Device	Description
						amplifier
174	LSPM	AUDIO	Passive	P_AUDIO	MC13783	Handset loudspeaker and alert amplifier
175	SPP	AUDIO	Output	P_AUDIO	MC13783	Handset earpiece speaker amplifier output
176	SPM	AUDIO	Output	P_AUDIO	MC13783	Handset earpiece speaker amplifier output
177	LSPL	AUDIO	Passive	P_AUDIO	MC13783	Low power output for discrete loudspeaker amplifier
178	HSL	AUDIO	Passive	P_AUDIO	MC13783	Headset left channel amplifier output
179	HSDET	AUDIO	Passive	P_AUDIO	MC13783	Headset sleeve detection input
180	HSPGFGS	AUDIO	Passive	P_AUDIO	MC13783	Headset phantom ground
181	HSR	AUDIO	Passive	P_AUDIO	MC13783	Headset right channel amplifier output
182	CDCOUT	AUDIO	Output	P_AUDIO	MC13783	Low power output for discrete amplifier
183	RXINL	AUDIO	Input	P_AUDIO	MC13783	General purpose receive input
184	RXINR	AUDIO	Input	P_AUDIO	MC13783	General purpose receive input
185	RXOUTL	AUDIO	Output	P_AUDIO	MC13783	Low power receive output
186	RXOUTR	AUDIO	Output	P_AUDIO	MC13783	Low power receive output
187	TXOUT	AUDIO	Output	P_AUDIO	MC13783	Buffered output of CEA-936-A microphone signal
188	TXIN	AUDIO	Input	P_AUDIO	MC13783	General purpose line level transmit input
189	MC2IN	AUDIO	Passive	P_AUDIO	MC13783	Headset microphone amplifier input
190	MC1RIN	AUDIO	Input	P_AUDIO	MC13783	Handset primary or right microphone amplifier input
191	MC1LIN	AUDIO	Input	P_AUDIO	MC13783	Handset secondary or left microphone amplifier input
192	MC2B	AUDIO	Output	P_AUDIO	MC13783	Headset microphone supply output
193	MC1RB	AUDIO	Output	P_AUDIO	MC13783	Handset primary or right microphone supply output

Pin	Name	Group	Type	Power Domain	Device	Description
194	MC1LB	AUDIO	Output	P_AUDIO	MC13783	Handset secondary or left microphone supply output

Table 4-12: Connector Sub-Symbol L - AUDIO

4.13 Sub Symbol M - ETH

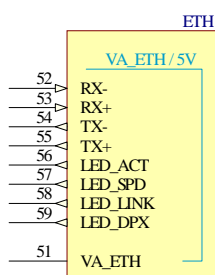


Figure 4-13: Connector Sub-Symbol M - ETH

Pin	Name	Group	Type	Power Domain	Device	Description
51	VA_ETH	ETH	Power	VA_ETH	LAN8700	Filter Supply Voltage
52	RX-	ETH	Input	VA_ETH	LAN8700	Recieve data -
53	RX+	ETH	Input	VA_ETH	LAN8700	Recieve data +
54	TX-	ETH	Output	VA_ETH	LAN8700	Transmit data -
55	TX+	ETH	Output	VA_ETH	LAN8700	Transmit data +
56	LED_ACT	ETH	Output	VA_ETH	LAN8700	ACTIVITY indication
57	LED_SPD	ETH	Output	VA_ETH	LAN8700	SPEED100 indication
58	LED_LINK	ETH	Output	VA_ETH	LAN8700	LINK ON indication
59	LED_DPX	ETH	Output	VA_ETH	LAN8700	DUPLEX indication

Table 4-13: Connector Sub-Symbol M - ETH

4.14 Sub Symbol N - SHIELD

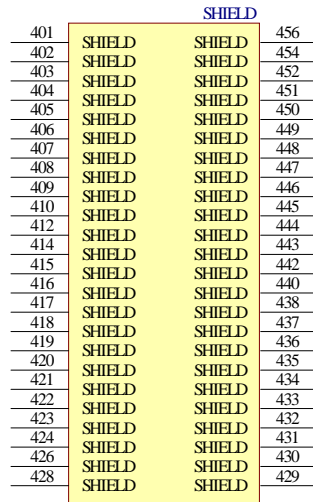


Figure 4-14: Connector Sub-Symbol N - SHIELD

Pin	Name	Group	Type	Power Domain	Device
401 – 456	SHIELD	SHIELD	Power	SHIELD	CM

Table 4-14: Connector Sub-Symbol N - SHIELD

4.15 Sub Symbol O – POWER_IN

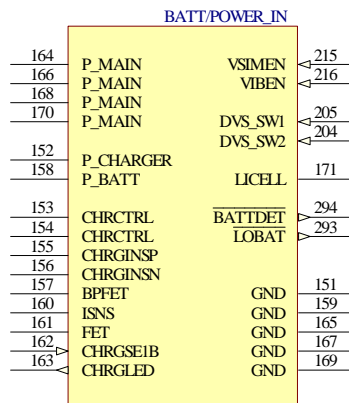


Figure 4-15: Connector Sub-Symbol O – POWER_IN

Pin	Name	Group	Type	Power Domain	Device	Description
151, 159, 165, 167, 169	GND	POWER IN	Power	Power	MC13783	Ground
153, 154	CHRCTRL	POWER IN	Passive	P_ATLAS	MC13783	Driver output for charger path

Pin	Name	Group	Type	Power Domain	Device	Description
						FETs M1 and M2
152	P_CHARGER	POWER IN	Power	Power	MC13783	Charger input
155	CHRGINSP	POWER IN	Passive	P_ATLAS	MC13783	Charge current sensing point
156	CHRGINSN	POWER IN	Passive	P_ATLAS	MC13783	Charge current sensing point
157	BPFET	POWER IN	Passive	P_ATLAS	MC13783	Driver output for dual path regulated BP FET M4
158	P_BATT	POWER IN	Power	Power	MC13783	Battery positive terminal
160	ISNS	POWER IN	Passive	P_ATLAS	MC13783	Battery current sensing point
161	FET	POWER IN	Passive	P_ATLAS	MC13783	Driver output for battery path FET M3
162	CHRGSE1B	POWER IN	Input	P_ATLAS	MC13783	Charger forced SE1 detection input
163	CHRGLED	POWER IN	Output	P_ATLAS	MC13783	Trickle LED driver output
164, 166, 168, 170	P_MAIN	POWER IN	Power	Power	MC13783	CM supply
171	LICELL	POWER IN	Power	Power	MC13783	Coincell supply input
204	DVS_SW2	POWER IN	Input	P_ATLAS	MC13783	Dynamic voltage scaling logic input for switcher 2
205	DVS_SW1	POWER IN	Input	P_ATLAS	MC13783	Dynamic voltage scaling logic input for switcher 1
215	VSIMEN	POWER IN	Input	P_ATLAS	MC13783	VESIM enable input
216	VIBEN	POWER IN	Input	P_ATLAS	MC13783	VVIB enable input
293	nLOBAT	POWER IN	Output	P_ATLAS	MC13783	Low battery indicator signal or end of life indicator signal
294	nBATDET	POWER IN	Output	P_ATLAS	MC13783	Battery thermistor presence detect output

Table 4-15: Connector Sub-Symbol O – POWER_IN

4.16 Sub Symbol P - CCM

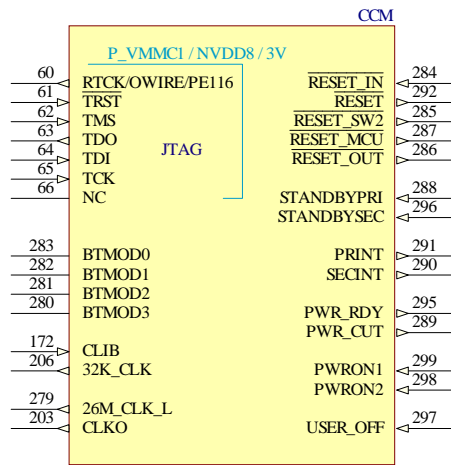


Figure 4-16: Connector Sub-Symbol P - CCM

Pin	Name	Group	Type	Power Domain	Device	Description
60	RTCK/OWIRE/PE116	JTAG	Output	P_VMMC1	i.MX27	JTAG Return Clock
61	nTRST	JTAG	Input	P_VMMC1	i.MX27	Test Reset Pin
62	TMS	JTAG	Input	P_VMMC1	i.MX27	Test Mode Select
63	TDO	JTAG	Output	P_VMMC1	i.MX27	Serial Output
64	TDI	JTAG	Input	P_VMMC1	i.MX27	Serial Input
65	TCK	JTAG	Input	P_VMMC1	i.MX27	Test Clock
66	NC					4.16.1
172	CLIB	CLK	Input	P_ATLAS	MC13783	Clock input for audio bus
203	CLKO	CLK	Output	P_ATLAS	i.MX27	Clock Out signal selected from internal clock signals
206	32K_CLK	CLK	Output	P_ATLAS	MC13783	32KHz Clock (2V75)
279	26M_CLK_L	CLK	Output	P_SW2	i.MX27	26MHz Clock (1V8)
280	BTMOD3	BOOTMODE	Passive	AVDD	i.MX27	System Boot Mode Select
281	BTMOD2	BOOTMODE	Passive	AVDD	i.MX27	System Boot Mode Select
282	BTMOD1	BOOTMODE	Passive	AVDD	i.MX27	System Boot Mode Select
283	BTMOD0	BOOTMODE	Passive	AVDD	i.MX27	System Boot Mode Select
284	nRESET_IN	RESET	Input	P_SW2	i.MX27	Master Reset

Pin	Name	Group	Type	Power Domain	Device	Description
285	nRESET_SW2	RESET	Output	P_SW2	MC13783	Reset output
286	nRESET_OUT	RESET	Output	P_VRF2	i.MX27	Reset_Out
287	nRESET_MCU	RESET	Output	P_SW2	MC13783	Reset for the processor
288	STANDBYPRI	INT	Input	P_ATLAS	MC13783	Standby input signal from primary processor
289	PWR_CUT	CTRL	Output	P_ATLAS	MC13783	Powerfail indicator output
290	SECINT	INT	Output	P_ATLAS	MC13783	Interrupt to processor
291	PRINT	INT	Output	P_ATLAS	MC13783	Interrupt to processor controlling the primary SPI bus
292	nRESET	RESET	Output	P_ATLAS	MC13783	Reset output
295	PWR_RDY	CTRL	Output	P_ATLAS	MC13783	Power ready signal after DVS and power gate transition
296	STANDBYSEC	INT	Input	P_ATLAS	MC13783	Standby input signal from secondary processor
297	USER_OFF	CTRL	Input	P_ATLAS	MC13783	Interrupt to processor
298	PWRON2	CTRL	Input	P_ATLAS	MC13783	Power on/off button connection
299	PWRON1	CTRL	Input	P_ATLAS	MC13783	Power on/off button connection

Table 4-16: Connector Sub-Symbol P - CCM

4.17 Sub Symbol Q - NFC

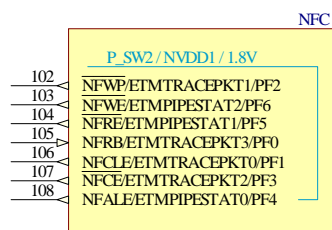


Figure 4-17: Connector Sub-Symbol Q - NFC

Pin	Name	Group	Type	Power Domain	Device	Description
102	nNFWP/ETMTRACEPKT1/PF2	NFC	Output	P_SW2	i.MX27	NFC Write Permit signal

Pin	Name	Group	Type	Power Domain	Device	Description
103	nNFWE/ETMPIPESTAT2/PF6	NFC	Output	P_SW2	i.MX27	NFC Write enable signal
104	nNFRE/ETMPIPESTAT1/PF5	NFC	Output	P_SW2	i.MX27	NFC Read enable signal
105	NFRB/ETMTRACEPKT3/PF0	NFC	Input	P_SW2	i.MX27	NFC read Busy signal
106	NFCLE/ETMTRACEPKT0/PF1	NFC	Output	P_SW2	i.MX27	NFC Command latch signal
107	nNFCE/ETMTRACEPKT2/PF3	NFC	Output	P_SW2	i.MX27	NFC Chip enable signal
108	NFALE/ETMPIPESTAT0/PF4	NFC	Output	P_SW2	i.MX27	NFC Address latch signal

Table 4-17: Connector Sub-Symbol Q - NFC

4.18 Sub Symbol R - GPIO

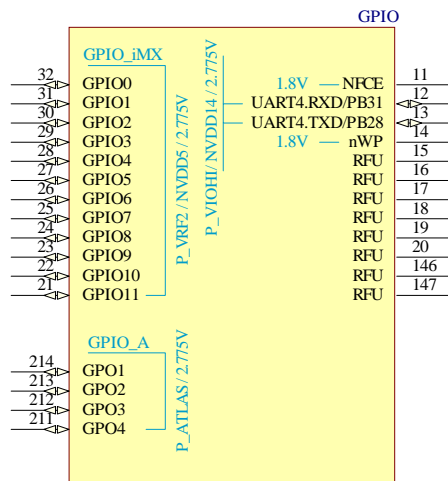


Figure 4-18: Connector Sub-Symbol R - GPIO

Pin	Name	Group	Type	Power Domain	Device	Description
11	NFCE	NFC	Passive	P_SW2	NAND	If high onboard NAND is disabled
12	UART4.RXD/PB31	UART	I/O	P_SW2	i.MX27	UART4_RXD, multiplexed with USB Host1 Receive Data Plus signal
13	UART4.TXD/PB28	UART	I/O	P_SW2	i.MX27	UART4_TXD, multiplexed with USB Host1 Transmit Data Minus signal
14	nWP	NOR	Passive	P_SW2	NOR	If low NOR is write protected

Pin	Name	Group	Type	Power Domain	Device	Description
15, 16, 17, 18, 19, 20, 146, 147	RFU					
21	GPIO11	GPIO	I/O	P_VRF2	i.MX27	PF18
22	GPIO10	GPIO	I/O	P_VRF2	i.MX27	PF13
23	GPIO9	GPIO	I/O	P_VRF2	i.MX27	PF14
24	GPIO8	GPIO	I/O	P_VRF2	i.MX27	PF8
25	GPIO7	GPIO	I/O	P_VRF2	i.MX27	PF10
26	GPIO6	GPIO	I/O	P_VRF2	i.MX27	PF17
27	GPIO5	GPIO	I/O	P_VRF2	i.MX27	PF16
28	GPIO4	GPIO	I/O	P_VRF2	i.MX27	PF7
29	GPIO3	GPIO	I/O	P_VRF2	i.MX27	PF19
30	GPIO2	GPIO	I/O	P_VRF2	i.MX27	PF20
31	GPIO1	GPIO	I/O	P_VRF2	i.MX27	PF11
32	GPIO0	GPIO	I/O	P_VRF2	i.MX27	PF12
211	GPO4	GPIO	I/O	P_ATLAS	ATLAS	General purpose output
212	GPO3	GPIO	I/O	P_ATLAS	ATLAS	General purpose output
213	GPO2	GPIO	I/O	P_ATLAS	ATLAS	General purpose output
214	GPO1	GPIO	I/O	P_ATLAS	ATLAS	General purpose output

Table 4-18: Connector Sub-Symbol R - GPIO

5 Example Schematics

The following schematics are suggestions of how to realize standard applications with the CM-i.MX27 Core Module. The following schematics represent a minimum configuration to get the CM-i.MX27 Core Module running.

5.1 Power

Figure 5-1: Shows the single-supply version without charger and battery.

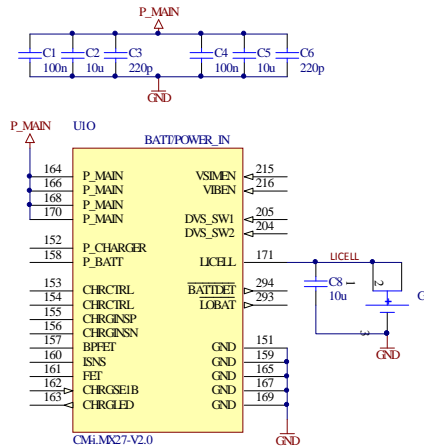


Figure 5-1: Single supply

Figure 5-2 shows the supply using the charger circuit and battery.

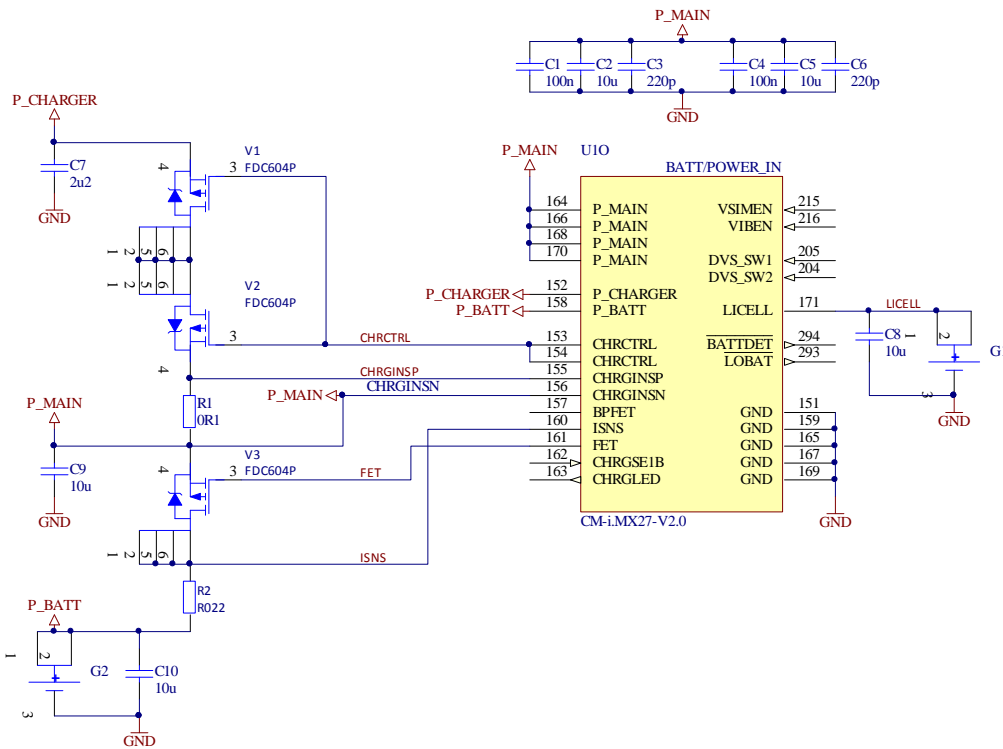


Figure 5-2: Supply with charger circuit

5.2 Boot Mode, Reset and JTAG

Figure 5-3: shows a boot configuration where the CM-i.MX27 is booting from the 8-Bit NAND Flash (2 Kbytes per page). For other boot modes refer to chapter 2.2. It also shows a simple reset configuration and how to wire a JTAG.

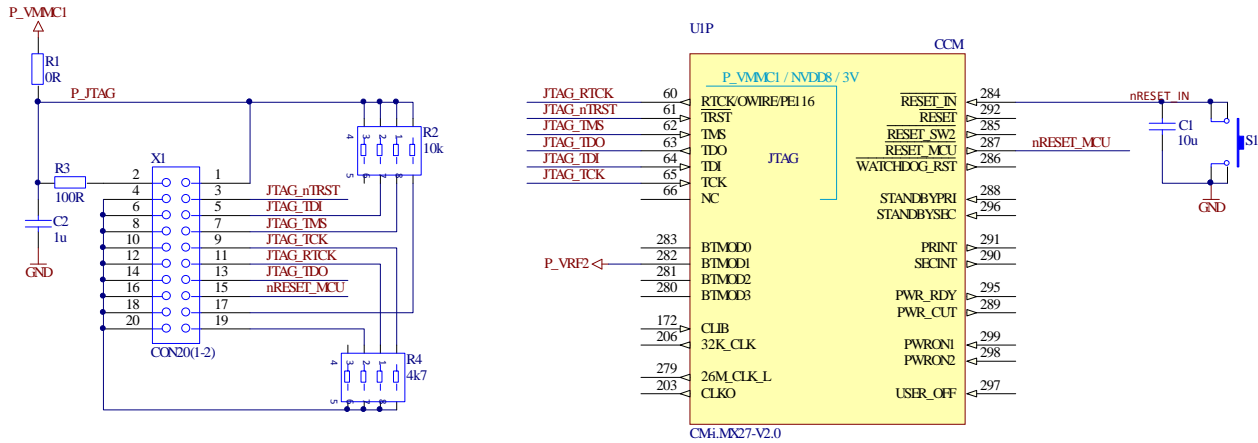


Figure 5-3: Boot Mode, Reset and JTAG

5.3 Further Application

For further applications refer to the DEV-i.MX27/35 schematic at the product home page.

<http://www.bluetechnix.com/goto/dev-i.mx27-35>

6 Design Verification

6.1 Schematic Design

6.1.1 Check Power Supply Requirements

- Is the power supply within the specified range?
- Is the ripple on P_CHARGER, P_MAIN, P_BATT, within the specified range?

6.1.2 Batteries

- Check the Li-Ion Battery voltage (only one cell Li-Ion Batteries are supported)
- Do you have a LICELL (coincell) in use? If no, add a 4u7 capacitor on the LICELL pin!
- Is the voltage range from the coincell within the spec?

6.1.3 Serial Communication

- Check RXD and TXD
- Check CTS and RTS if used
- Are level shifters needed? (I/O voltage level 2.8V!)

6.1.4 USB OTG

- D+ and D- correct?
- ID pin in use?
- External power MOSFET needed?
- ESD protection?

6.1.5 Ethernet

- Termination resistors on RX/TX lines?
- Transformer in specified range?

6.1.6 Boot Modes

- Are the boot mode pins set correctly for boot up?
- Is it possible to use the Bootstrap boot up mode (e.g. for usage in conjunction with the ATK tool)?

6.2 PCB Layout

- Add a ground plane underneath the Core Module to reduce interference
- Do not place any high components underneath the Core Module
- To reduce interference place ceramic decoupling capacitors on the power supplies near the balls/pins (at least 100nF and 220pF).
- Check if the USB lines (D+/D-) have the correct impedance and that they are routed as differential line pairs!
- Check if the Ethernet lines (Rx/Tx) have the correct impedance and that they are routed as differential line pairs!

7 Grounding Metal Covers

The Core Module has a ground ring around the PCB outlines which is connected directly to the GND plane for reducing EMI. Bluetechnix takes no warranty for damages on the Core Module caused by soldering a metal case on our Core Module!

8 Mechanical Stress

Note that excessive twisting while inserting or withdrawing the CM-i.MX27C will damage the connectors.

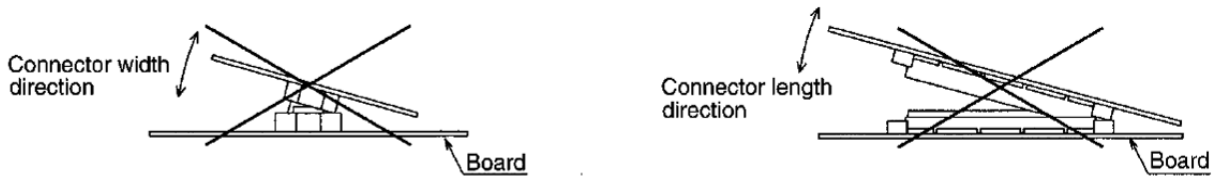


Figure 8-1: Unplugging the Core Module

9 Package Information

9.1 Embossed Carrier Tape Dimensions

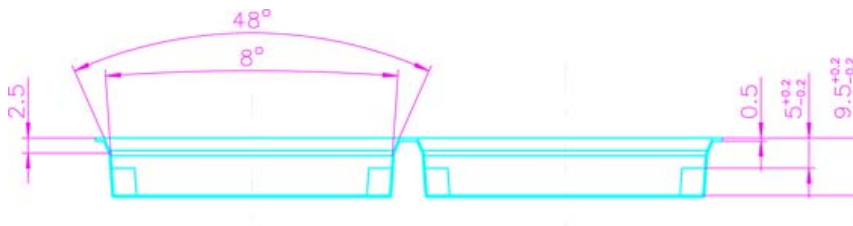


Figure 9-1: Blister side view

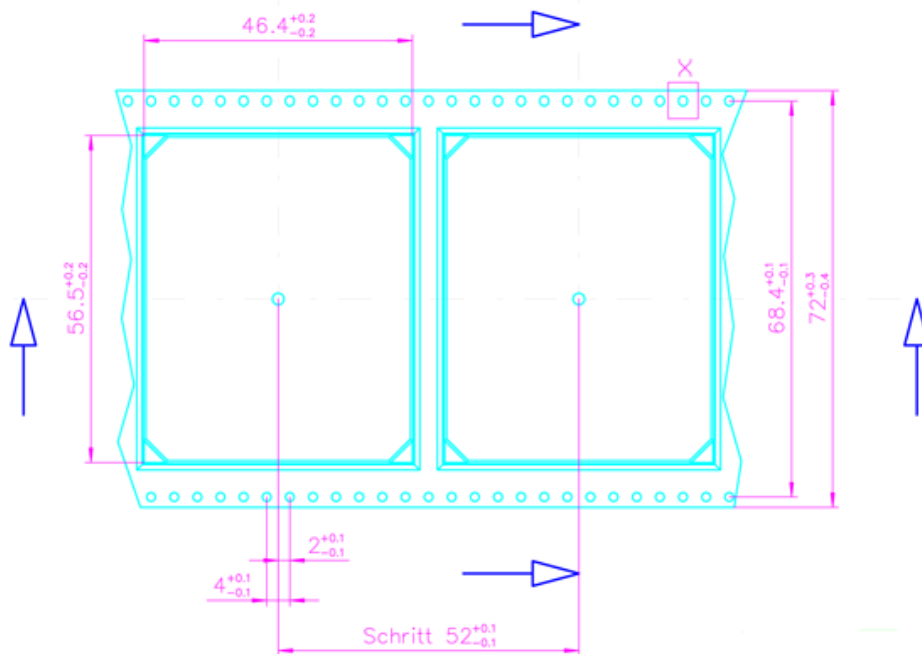


Figure 9-2: Blister top view

9.2 Storage

Shelf life in a sealed bag is 12 months at <40°C and <90% relative humidity.

9.3 Handling

The Core Modules are shipped on tape-and-reel in a hermetically sealed package which includes a humidity indicator card.

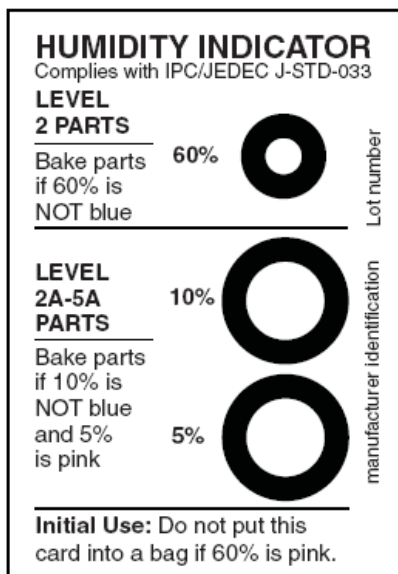


Figure 9-3: Example Humidity Indicator Card

10 Anomalies

For the latest up-to-date information about this product, please consult the product homepage:

<http://www.bluetechnix.com/goto/cm-i.MX27c>

11 Order Information

Product Code	Order Code
CM-i.MX27C	100-1411

Table 11-1: Order Code

12 Product Changes

For the latest information regarding product changes, please consult the product homepage:

<http://www.bluetechnix.com/goto/cm-i.MX27c>

Version	Changes
V2.1	Complete Redesign
V1.2	No changes, new production only
V1.1	First Release

Table 12-1: Product Changes

13 Document Revision History

Version	Date	Document Revision
1	08.05.2010	First Version

Table 13-1: Revision History

14 List of abbreviations

BGA	Ball Grid Array
USB	Universal Serial Bus
EMI	External Memory Interface
CSPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
I ² C	Inter Integrated Circuit Connection
UART	Universal Asynchronous Receiver/Transmitter
USB OTG	USB On-The-Go
USB FS/HS	USB Full Speed / High Speed
IrDA	Infrared Data Association
MMC	Multi Media Card
SD	Secure Digital Card
PCMCIA	Personal Computer Memory Card International Association
CF	Compact Flash
SIM	Subscriber Identification Module
ATA	Advanced Technology Attachment
SDRAM	Synchronous Dynamic Random Access Memory
DDR	Double Data Rate SDRAM
NANDF	NAND Flash
PSRAM	Pseudostatic RAM
SDMA	Smart Direct Memory Access
PWM	Pulse-Width Modulation
WD	Watchdog
RTC	Real-Time Clock
GPIO	General Purpose Input/Output
RAM	Random Access Memory
ROM	Read-Only Memory
MPEG	Moving Picture Experts Group
JTAG	Joint Test Action Group (IEEE 1149.1 Standard)
ETM	Embedded Trace Macrocell (ARMs JTAG Extension)
DVS	Dynamic Voltage Scaling
RF	Radio Frequency
ADC	Analog-Digital Converter or Asynchronous Display Controller
PLL	Phase-Locked Loop
OV	Over-Voltage
UV	Under-Voltage
RST	Reset
LCD	Liquid Crystal Display
LED	Light-Emitting Diode
MCP	Multi-Chip Product
FPGA	Field-Programmable Gate Array
PDA	Personal Digital Assistant
NTC	Negative Temperature Coefficient Resistor

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