

# Hardware User Manual

**TCM-BF518 V1.x**

*...maximum performance at minimum space*

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#### **Information**

For further information on technology, delivery terms and conditions and prices please contact Bluetechnix (<http://www.bluetechnix.com>).

#### **Warning**

Due to technical requirements components may contain dangerous substances.

## Blackfin<sup>®</sup> Core Modules

### [TCM-BF518-C-C-Q25S32F2 \(TCM-BF518\)](#)

The Tiny Core Module TCM-BF518 is powered by Analog Devices' single core ADSP-BF518 processor; up to 400MHz, 32MB SDRAM, up to 8MB flash. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.

### [ACM-BF525C-C-C-Q25S64F4N1024](#)

The Core Module ACM-BF525C is optimized for audio applications and performance. It is based on the high performance ADSPBF525C from Analog Devices. It addresses 64MByte SDRAM via its 16bit wide SDRAM bus, has an onboard NOR-flash of 4MByte and a NAND-flash with 1024MByte.

### [CM-BF527-C-C-Q50S32F8 \(CM-BF527\)](#)

The Core Module CM-BF527 is powered by Analog Devices' single core ADSP-BF527 processor; key features are USB OTG 2.0 and Ethernet. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.

### [CM-BF533-C-C-Q25S32F2 \(CM-BF533\)](#)

The Core Module CM-BF533 is powered by Analog Devices' single core ADSP-BF533 processor; up to 600MHz, 32MB SDRAM, 2MB flash, 2x60 pin expansion connectors at a size of 36.5x31.5mm.

### [TCM-BF537-C-I-Q25S32F8 \(TCM-BF537\)](#)

The Tiny Core Module TCM-BF537 is powered by Analog Devices' single core ADSP-BF537 processor; up to 500MHz, 32MB SDRAM, 8MB flash, a size of 28x28mm, 2x60 pin expansion connectors, Ball Grid Array or Border Pads for reflow soldering, industrial temperature range -40°C to +85°C.

### [CM-BF537-C-C-Q25S32F4 \(CM-BF537E\)](#)

The Core Module CM-BF537 is powered by Analog Devices' single core ADSP-BF537 processor; up to 600MHz, 32MB SDRAM, 4MB flash, integrated TP10/100 Ethernet physical transceiver, 2x60 pin expansion connectors at a size of 36.5x31.5mm.

### [CM-BF537-C-C-Q30S32F4-U \(CM-BF537U\)](#)

The Core Module CM-BF537 is powered by Analog Devices' single core ADSP-BF537 processor; up to 600MHz, 32MB SDRAM, 4MB flash, integrated USB 2.0 Device, 2x60 pin expansion connectors at a size of 36.5x31.5mm.

### [CM-BF548-C-C-Q25S64F8 \(CM-BF548\)](#)

The Core Module CM-BF548 is characterized by its numerous peripheral interfaces, its performance in combination with its high speed memory interface (DDR). Key features are 533MHz, 64MB DDR SD-RAM (266MHz), and 8MB flash.

### [CM-BF561-C-C-Q25S64F8 \(CM-BF561\)](#)

The Core Module CM-BF561 is powered by Analog Devices' dual core ADSP-BF561 processor; up to 2x 600MHz, 64MB SDRAM, 8MB flash, 2x60 pin expansion connectors at a size of 36.5x31.5mm.

### [eCM-BF561-C-C-Q25S128F32 \(eCM-BF561\)](#)

The Core Module CM-BF561 is powered by Analog Devices' dual core ADSP-BF561 processor; up to 2x 600MHz, 128MB SDRAM, 8MB flash, 2x100 pin expansion connectors and a size of 44x33mm.

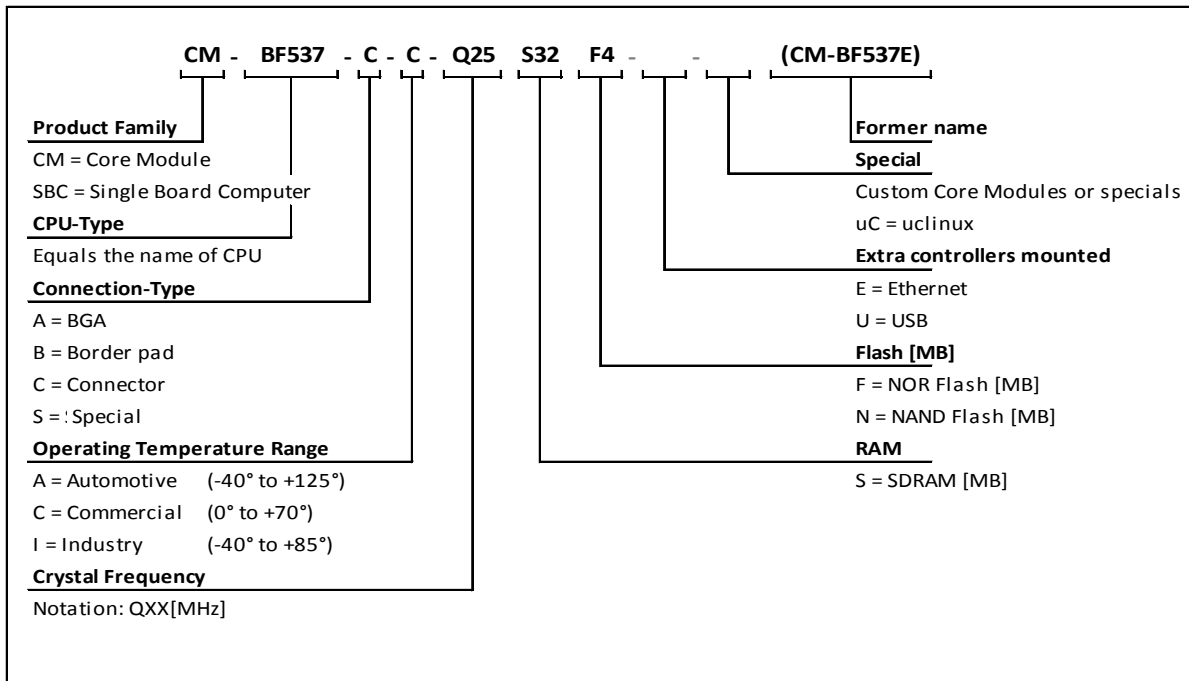
## Core Module naming information

The idea is to put more Core Module specific technical information into the product name. New Core Module names will have following technical information covered in their names.

- Product Family,
- CPU-Type,
- Connection-Type,
- Operating Temperature Range,
- Crystal Frequency [MHz],
- RAM [MB],
- Flash [MB],
- External Controllers
- Optional
  - Special and/or
  - Former name

That expands of course the name but allows the customer to get the most important Core Module specific information at the first sight. Have a look at the example below to get an idea of the new Core Module names.

### Example CM-BF537-C-C-Q25S32F4 (CM-BF537E)



## Blackfin® Development Boards

### [ADEV-BF52xC](#)

Feature rich, low cost embedded audio development platform which supports Audio Core Modules (ACM). The form factor of the ADEV-BF52xC allows easy integration of the board into OEM products. Dedicated interfaces such as USB2.0, Line In/Out, headphone out and an onboard silicon microphone turn the ADEV-BF52xC into a full-featured development platform for most embedded audio applications in commercial areas.

### [DEV-BF5xxDA-Lite](#)

Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including an USB-Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including a VDSP++ Evaluation Software License.

### [DEV-BF548-Lite](#)

Low-cost development board with a socket for Bluetechnix' CM-BF548 Core Module. Additional interfaces are available, e.g. an SD-Card, USB and Ethernet.

### [DEV-BF548DA-Lite](#)

Get ready to program and debug Bluetechnix CM-BF548 Core Module with this tiny development platform including an USB-Based Debug Agent. The DEV-BF548DA-Lite is a low-cost starter development system including a VDSP++ Evaluation Software License.

### [eDEV-BF5xx](#)

Feature rich, low cost rapid development platform which provides all interfaces on dedicated connectors and has all Core Module pins routed to solder pads which easily can be accessed by the developers. The eDEV-BF5xx supports the latest debugging interface from Analog Devices - ADI-SADA (Analog Devices Stand Alone Debug Agent).

### [EVAL-BF5xx](#)

Tiny, low cost embedded platform which supports Bluetechnix powerful Blackfin® based Core Modules. The form factor (75x75mm) of the EVAL-BF5xx allows easy integration of the board into OEM products. Dedicated interfaces such as USB2.0, SD-card slot, CAN interface connectors and of course Ethernet, turn the EVAL-BF5xx into a full-featured evaluation platform for most embedded applications.

### [Extender boards](#)

Extender boards (EXT-BF5xx) are expanding the development and evaluation boards by several interfaces and functionalities. Targeted application areas are: audio/video processing, security and surveillance, Ethernet access, positioning, automation and control, experimental development and measuring.

Note! Bluetechnix is offering tailored board developments as well.

## 1 Introduction

The Tiny Core Module TCM-BF518 is optimized for performance and size. The module integrates processor, RAM, flash and power supply at a size of 28x28mm! It is based at the high performance ADSP-BF518 from Analog Devices. The Core Module is designed for commercial usage. It addresses 32MByte SDRAM via its 16bit wide SDRAM bus and has an on-board NOR-flash of 8MByte.

### 1.1 Overview

Figure 1-1 shows the main components of the Core Module TCM-BF518.

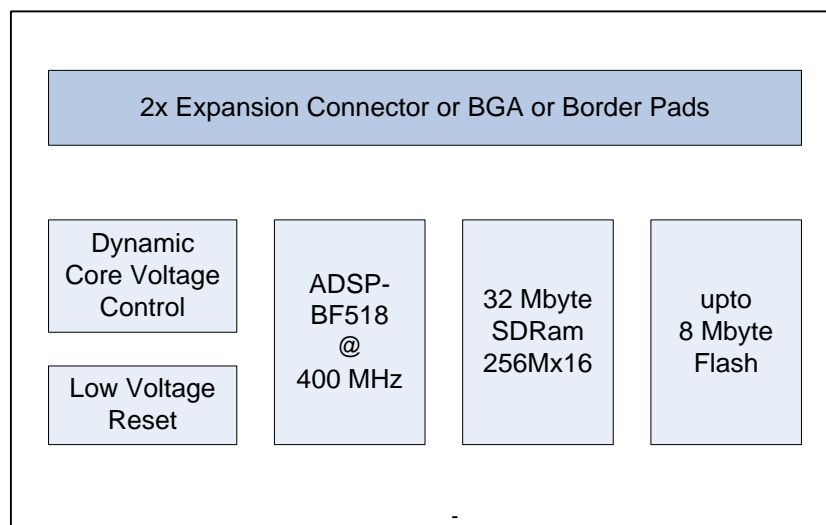


Figure 1-1: Main components of the TCM-BF518 Core Module

### 1.2 Key Features

- **Blackfin Processor BF518 from Analog Devices**
  - ADSP-BF518KSWZ, 400MHz (0°C to +70°C)
- **32 MB SDRAM**
  - SDRAM Clock up to 133MHz
  - MT48LC16M16A2BG-7 (16Mx16, 256Mbit at 3.3 V)
- **8 MB of Byte Addressable Flash**
  - PF48F2000P0ZBQ0S (32Mx16, 2MByte directly addressable; all 8MByte addressable using external connection of A2x lines via GPIOs)
  - Additional flash memory upon request: It can be connected through the expansion board as parallel flash using asynchronous chip select lines or as SPI flash.
- **Low Voltage Reset Circuit**
  - Resets the module if the supply voltage drops below 2.93V.
- **Core Voltage Control**

- Core voltage 1.35V (0.95V - 1.5V)
- **Peripherals available on all Core Module versions**
  - Power Supply
  - SPORT 0
  - JTAG
  - UART0/UART1
  - TWI (I2C compatible)
  - SPI (Serial Port Interface)
  - PPI (Parallel Port Interface)
  - Boot Mode Pins
  - GPIO's
- **Peripherals only available on the Connector and BGA version**
  - Data Bus
  - Address Bus
  - Further GPIO's
  - Memory Control Signals

### 1.3 Highlights

- ADSP BF518 DSP,
- 32 MByte SD RAM up to 133Mhz
- 2 MByte Flash
- Very small design (28 x 28 mm)
- Low Power Designs
- Commercial Core Module (0 to +70°C)

### 1.4 Applications

- VoIP
- Industrial Control
- Motor Control
- Femto Cells
- Networked Audio
- Instrumentation

### 1.5 Further Information

Further information, and document updates are available on the product homepage:  
<http://www.bluetechnix.com/goto/tcm-bf518>

## 2 General Description

### 2.1 Functional Description

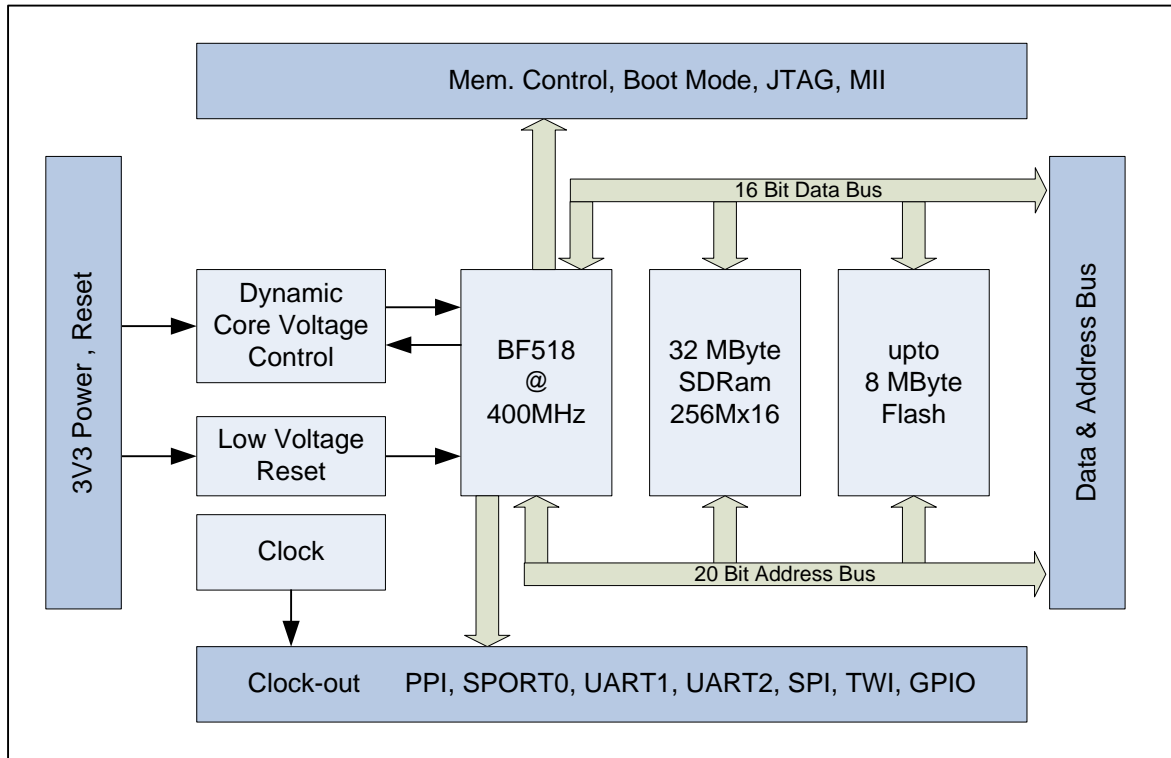


Figure 2-1: Detailed block diagram

Figure 2-1 shows a detailed block diagram of the TCM-BF518 module. Beside the SDRAM and a few other control pins, the TCM-BF518 has most pins of the Blackfin processor on its two 60-pin connectors, or it's BGA, or its Border Pads.

A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V for at least 140ms.

### 2.2 Boot Mode

By default the boot mode = 000 (BMODE2 = Low, BMODE1 = Low, BMODE0=Low). All BMODE pins have on board pull down resistors.

Switch Settings BMODE[2..0]	Boot Mode	Description
000	0	Idle - No boot
001	1	Boot from 8- or 16-bit external flash memory
010	2	Boot from internal SPI memory
011	3	Boot from external SPI memory (EEPROM or flash)
100	4	Boot from SPI0 host
101	5	Boot from OTP memory
110	6	Boot from SDRAM

111 7 Boot from UART0

Table 2-1: TCM-BF518 boot modes

Connect BMODE0 to V<sub>CC</sub> and leave both BMODE1 and BMODE2 pins open to adjust Boot Mode 1. This is the default boot mode for BLACKSheep® OS.

## 2.3 Memory Map

### 2.3.1 Core Module Memory

Type	Start Address	End Address	Size	Comment
<b>FLASH</b> *)	0x20000000	0x201FFFFFF	2MByte	¼ of 8MB Flash, PF48F2000P0ZBQ0S
<b>SD-RAM</b>	0x00000000	0x01FFFFFF	32MByte	16 bit Bus Micron,MT48LC16M16A2FG

Table 2-2: Memory map

\*) Be aware that you have to unlock the flash before starting an erase process!

### 2.3.2 Externally Addressable Memory (on connector)

The Blackfin processor can address a maximum of 1MB with a single asynchronous memory bank. On this module, each 2MB segment of flash is addressed using 2 asynchronous memory banks. In order to be able to use more than 2MB without using more than 2 banks, GPIOs can be used to select which 2MB section of the FLASH is visible in the memory window of the Blackfin processor. This frees up the remaining banks for the user. Address lines A20 - A24 of the flash are available on the connectors and can be connected to free GPIOs.

Bank	Start Address	End Address	Size	Comment
<b>0</b>	0x20000000	0x200FFFFFF	1MB	(Addresses FLASH)
<b>1</b>	0x20100000	0x201FFFFFF	1MB	(Addresses FLASH)

Table 2-3: Externally addressable memory

**NOTE: Pins FA20 to FA24** - These pins are the address lines A20 (FA20) to A24 (FA24) of the Intel P30 Flash and are pulled down by default.

### 3 Specifications

#### 3.1 Electrical Specifications

##### 3.1.1 Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IN}$	Input supply voltage	3.15	3.3	3.45	V
$I_{3V3}$	3.3V current		<b>TBD</b>		mA
$V_{OH}$	High level output voltage	2.4			V
$V_{OL}$	Low level output voltage			0.4	V
$I_{IH}$	IO input current			10	$\mu$ A
$I_{OZ}$	Three state leakage current			10	$\mu$ A
$I_{TYP}$	$V_{IN}$ current in with core running at 400 MHz		<b>TBD</b>		mA
$I_{RTC}$	$V_{RTC}$ current		20		$\mu$ A
$f_{CCLK}$	Core clock frequency		400		MHz

Table 3-1: Electrical characteristics

##### 3.1.2 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
$V_{IO}$	Input or output voltage	-0.5	3.8	V
$V_{IN}$	Input supply voltage	3.0	5.5	V
$I_{OH}/I_{OL}$	Current per pin	0	10	mA
$T_{AMB}$	Ambient temperature	-40	85	$^{\circ}$ C
$T_{STO}$	Storage temperature	-55	150	$^{\circ}$ C
$T_{SLD}$	Solder temperature for 10 seconds		260	$^{\circ}$ C
$\phi_{AMB}$	Relative ambient humidity		90	%

Table 3-2: Absolute maximum ratings

##### 3.1.3 ESD Sensitivity



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## 4 Connector Description

### 4.1 Connector X1

Pin No.	Signal Name	Type	Function
1	PH2/RSCLK1/SPI1SCK/RSI DATA6	I/O	GPIO/SPORT1 Rx Clock/SPI1 Clock/RSI Data 6
2	PH0/DR1PRI/SPI1SS/RSI_DATA4	I/O	GPIO/SPORT1 Primary Rx Data/SPI1 Device Select/RSI Data 4
3	PH5/TSCLK1/ARDY/PTP_EXT_CLKIN/CDG	I/O	GPIO/SPORT1 Tx Clock/Asynchronous Memory Hardware Ready Control/ External Clock for PTP TSYNC/Counter Down Gate
4	PH3/DT1PRI/SPI1MOSI/RSI DATA7	I/O	GPIO/SPORT1 Primary Tx Data/SPI1 Master Out Slave In/RSI Data 7
5	CLKBUF	I/O	Buffered XTAL Output
6	SDA	I/O	TWI Serial Data
7	PG4/RSCLK0/RSI_DATA1/TMR5/TACI5	I/O	GPIO/SPORT0 Rx Clock/RSI Data 1/Timer 5/Timer5 Alternate Capture Input
8	PG1/ERxER/DMAR1/PWM CH	I/O	GPIO/Ethernet MII or RMIIL Receive Error/DMA Req 1/PWM CH Out
9	Vin 3V3	Power	
10	Vin 3V3	Power	
11	PF0/ETxD2/PPI D0/SPI1SEL2/TACLK6	I/O	GPIO/Ethernet MII Transmit D2/PPI Data 0/SPI1 Slave Select 2/Timer6 Alternate Clock
12	PF2/ETxD3/PPI D2/PWM AL	I/O	GPIO/Ethernet Transmit D3/PPI Data 2/PWM AL Output
13	PF4/ERxCLK/PPI D4/PWM BL/TACLK1	I/O	GPIO/Ethernet MII Receive Clock/PPI Data 4/PWM BL Out/Timer1 Alternate CLK
14	PF6/COL/PPI D6/PWM CL/TACI1	I/O	GPIO/Ethernet MII Collision/PPI Data 6/PWM CL Out/Timer1 Alternate Capture Input
15	PF8/MDC/PPI D8/SPI1SEL4	I/O	GPIO/Ethernet Management Channel Clock/PPI Data 8/SPI1 Slave Select 4
16	PF10/ETxD0/PPI D10/TMR3	I/O	GPIO/Ethernet MII or RMIIL Transmit D0/PPI Data 10/Timer 3
17	PF12/ETxD1/PPI D12/PWM AL	I/O	GPIO/Ethernet MII Transmit D1/PPI Data 12/PWM AL Output
18	PF14/ETxEN/PPI D14/PWM BL	I/O	GPIO/Ethernet MII Transmit Enable/PPI Data 14/PWM BL Out
19	PG15/SPI0SEL2/PPIFS3/AMS3	I/O	GPIO/SPI0 Slave Select 2/PPI Frame Sync3/Asynchronous Memory Bank Select 3
20	PG6/TFS0/RSI_DATA3/TMR0/PPIFS1	I/O	GPIO/SPORT0 Tx Frame Sync/RSI Data 3/Timer0/PPI Frame Sync1
21	PG8/TSCLK0/RSI_CLK/TMR6/TACI6	I/O	GPIO/SPORT0 Tx Clock/RSI Clock/Timer 6/Timer6 Alternate Capture Input
22	PH7/DR1SEC/UART1RX/TMR7/TACI2	I/O	GPIO/SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input
23	PG10/DR0SEC/UART0RX/TACI4	I/O	GPIO/SPORT0 Secondary Rx Data/UART0 Receive/Timer4 Alternate Capture Input

Pin No.	Signal Name	Type	Function
24	PG14/SPI0MOSI/TMR1/PPIFS2/PWM TRIP	I/O	GPIO/SPI0 Master Out Slave In/Timer 1/PPI Frame Sync2/PWM Trip/PTP Auxiliary Snapshot Trigger Input
25	PG12/SPI0SCK/PPICLK/TMRCLK/PTP_PPS	I/O	GPIO/SPI0 Clock/PPI Clock/External Timer Reference/PTP Pulse Per Second Out
26	Bmode0	I - 10k pull down	Boot Mode 0
27	GND	Power	
28	TCK	I - 10k pull up	JTAG Clock
29	TDI	I - 10k pull up	JTAG Data In
30	TRST	I - 4k7 pull down	JTAG Reset
31	EMU	O	JTG Emulation Output
32	TMS	I - 10k pull up	JTAG Mode Select
33	TDO	O	JTAG Data Out
34	Bmode2	I - 10k pull down	Boot Mode 2
35	nc		
36	Bmode1	I - 10k pull down	Boot Mode 1
37	PG13/SPI0MISO4/TMR0/PPIFS1/	I/O	GPIO/SPI0 Master In Slave Out/Timer0/PPI Frame Sync1/PTP Clock Out
38	PG9/DT0SEC/UART0TX/TMR4	I/O	GPIO/SPORT0 Secondary Tx Data/UART0 Transmit/Timer 4
39	PG11/SPI0SS/AMS2/SPI1SEL5/TACLK2	I/O	GPIO/SPI0 Slave Device Select/Asynchronous Memory Bank Select 2/SPI1 Slave Select 5/Timer2 Alternate CLK
40	PH6/DT1SEC/UART1TX/SPI1SEL1/CZM	I/O	GPIO/SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker
41	PG5/RFS0/RSI_DATA2/PPICLK/TMRCLK	I/O	GPIO/SPORT0 Rx Frame Sync/RSI Data 2/PPI Clock/External Timer Reference
42	PG7/DT0PRI/RSI_CMD/TMR1/PPIFS2	I/O	GPIO/SPORT0 Tx Primary Data/RSI Command/Timer 1/PPI Frame Sync2
43	PF15/RMII PHYINT/PPI D15/PWM_SYNCA	I/O	GPIO/Ethernet MII PHY Interrupt/PPI Data 15/Alternate PWM Sync
44	PF13/ERxD1/PPI D13/PWM BH	I/O	GPIO/Ethernet MII or RMII Receive D1/PPI Data 13/PWM BH Output
45	PF11/ERxD0/PPI D11/PWM AH/TACI3	I/O	GPIO/Ethernet MII Receive D0/PPI Data 11/PWM AH output /Timer3 Alternate Capture Input
46	PF9/MDIO/PPI D9/TMR2	I/O	GPIO/Ethernet Management Channel Serial Data/PPI Data 9/Timer 2
47	PF7/SPI0SEL1/PPI D7/PWMSYNC	I/O	GPIO/SPI0 Slave Select 1/PPI Data 7/PWM Sync
48	PF5/ERxDV/PPI D5/PWM CH/TACI0	I/O	GPIO/Ethernet MII Receive Data Valid/PPI Data 5/PWM CH Out /Timer0 Alternate Capture Input
49	PF3/ERxD3/PPI D3/PWM BH/TACLK0	I/O	GPIO/Ethernet MII Data Receive D3/PPI Data 3/PWM BH Output/Timer0 Alternate Clock
50	PF1/ERxD2/PPI D1/PWM AH/TACLK7	I/O	GPIO/Ethernet MII Receive D2/PPI Data 1/PWM AH Output/Timer7 Alternate Clock
51	GND	Power	
52	GND	Power	

Pin No.	Signal Name	Type	Function
53	PG0/MIICRS/RMIICRS/HWAIT 3/SPI1SEL3	I/O	GPIO/Ethernet MII or RMIIC Carrier Sense or RMIIC Data Valid/HWAIT/SPI1 Slave Select3
54	PG2/MIITxCLK/RMIIREF_CLK/DMAR0/PWM CL	I/O	GPIO/Ethernet MII or RMIIC Reference Clock/DMA Req 0/PWM CL Out
55	PG3/DR0PRI/RSI_DATA0/SPI0SEL5/TACLK3	I/O	GPIO/SPORT0 Primary Rx Data/RSI Data 0/SPI0 Slave Select 5/Timer3 Alternate CLK
56	SCL	O	TWI Serial Clock
57	PH6/DT1SEC/UART1TX/SPI1SEL1/CZM	I/O	GPIO/SPORT1 Secondary Tx Data/UART1 Transmit/SPI1 Slave Select 1 /Counter Zero Marker
58	PH4/TFS1/AOE/SPI0SEL3/CUD	I/O	GPIO/SPORT1 Tx Frame Sync/Asynchronous Memory Output Enable/SPI0 Slave Select 3/Counter Up Direction
59	PH7/DR1SEC/UART1RX/TMR7/TAC12	I/O	GPIO/SPORT1 Secondary Rx Data/UART1 Receive/Timer 7/Timer2 Alternate Clock Input
60	PH1/RFS1/SPI1MISO/RSI_DATA5	I/O	GPIO/SPORT1 Rx Frame Sync/SPI1 Master In Slave Out/RSI Data 5

Table 4-1: Connector description X1

## 4.2 Connector X2

Pin No.	Signal Name	Type	Function
61	A1	O	Address Bus
62	A3	O	Address Bus
63	A5	O	Address Bus
64	A7	O	Address Bus
65	A9	O	Address Bus
66	A11	O	Address Bus
67	A13	O	Address Bus
68	A15	O	Address Bus
69	A17	O	Address Bus
70	A19	O	Address Bus
71	A\B\E1\	O	Byte Enable
72	FA20	I - 10k pull down	Address Bus
73	FA23	I - 10k pull down	Address Bus
74	VDD_OTP	I/O	OTP Power Supply
75	nc	-	-
76	PH5/ARDY	I/O	Hardware Ready Control
77	nc	-	-
78	CLKOUT	O	Clock Output
79	GND	Power	
80	PG15/AMS3	O	Bank Select
81	A\W\E\	O	Write Enable
82	N\M\I\	I	Nonmaskable Interrupt
83	D0	I/O	Data Bus
84	D2	I/O	Data Bus
85	D4	I/O	Data Bus
86	D6	I/O	Data Bus
87	D8	I/O	Data Bus

Pin No.	Signal Name	Type	Function
88	D10	I/O	Data Bus
89	D12	I/O	Data Bus
90	D14	I/O	Data Bus
91	D15	I/O	Data Bus
92	D13	I/O	Data Bus
93	D11	I/O	Data Bus
94	D9	I/O	Data Bus
95	D7	I/O	Data Bus
96	D5	I/O	Data Bus
97	D3	I/O	Data Bus
98	D1	I/O	Data Bus
99	RE\S/E\T\	I/O	Reset
100	PH4/AOE	I/O	Output Enable
101	A\R\E\	O	Read Enable
102	PG11/AMS2	I/O	Bank Select
103	VDD-RTC	Power	
104	nc	-	-
105	nc	-	-
106	nc	-	-
107	nc	-	-
108	FA22	I - 10k pull down	Address Bus
109	FA24	I - 10k pull down	Address Bus
110	FA21	I - 10k pull down	Address Bus
111	A\B\E\0\	O	Byte Enable
112	A18	O	Address Bus
113	A16	O	Address Bus
114	A14	O	Address Bus
115	A12	O	Address Bus
116	A10	O	Address Bus
117	A8	O	Address Bus
118	A6	O	Address Bus
119	A4	O	Address Bus
120	A2	O	Address Bus

Table 4-2: Connector description X2

## 5 Application Information

### 5.1 Supply Voltage Decoupling

### 5.2 Reset circuit

The reset signal of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 5-1.

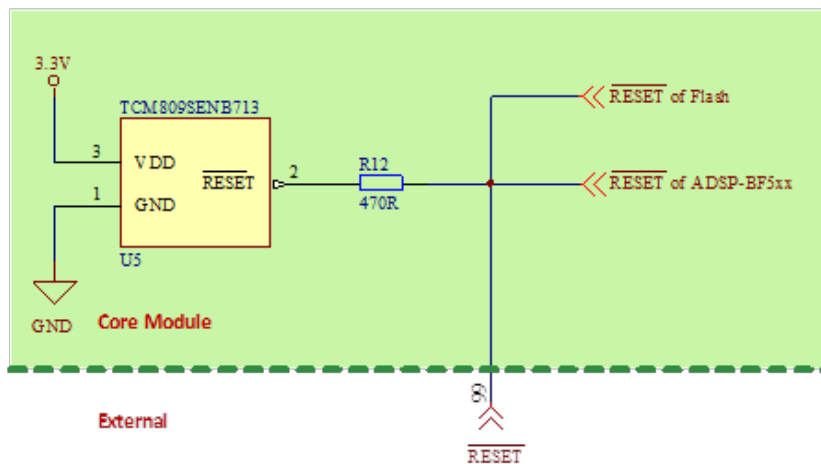


Figure 5-1: Schematic of reset circuit on the Core Module

If reset inputs of other devices are connected to the external RESET pin, an additional driver should be used.

### 5.3 Application Example Schematics

#### 5.3.1 Connecting a Physical Ethernet Chip

The ADSP-BF518 from Analog Devices already integrates the Ethernet functionality. In order to use the Ethernet feature, a Physical Ethernet chip needs to be connected to the TCM-BF518 Core Module.

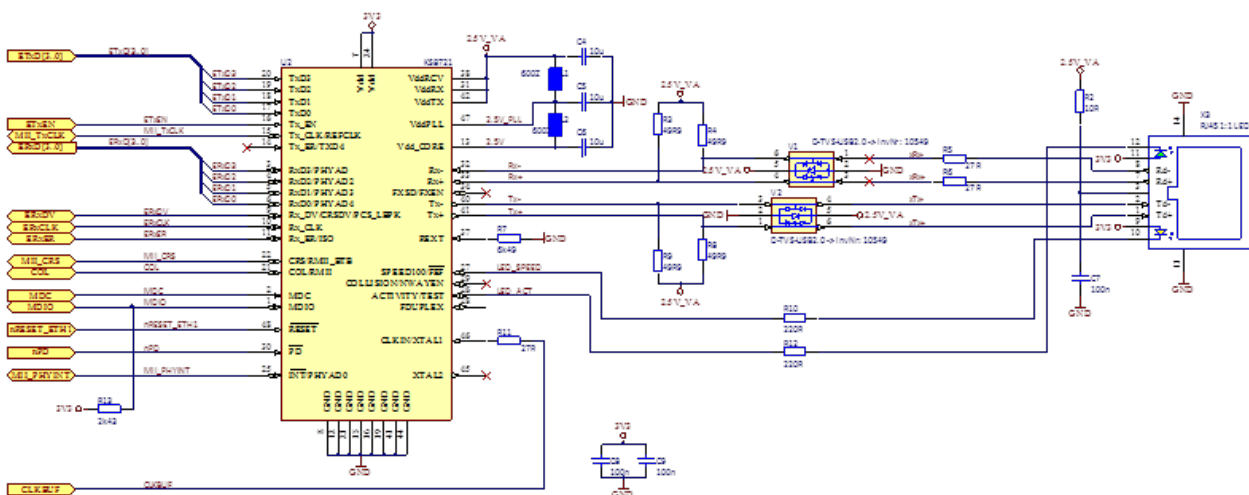


Figure 5-2: Connection of the Physical Ethernet chip with the Core Module

Designator	Value	Part Number	Description	Quantity
<b>C1, C7, C8, C9, C10, C11, C12</b>	100n	2238 246 19876	Capacitor non-polarized	7
<b>C2, C4, C5, C6</b>	10u	C0805C106K9PAC	Capacitor non-polarized	4
<b>C13</b>	100p	2238 867 15101	Capacitor non-polarized	1
<b>L1</b>	2200Z	742792693	Ferrite	1
<b>R2</b>	10R	MC 0.063W 0603 1% 10R	Resistor	1
<b>R3, R4, R8, R9</b>	49R9	MC 0.063W 0603 1% 49R9	Resistor	4
<b>R7</b>	6k49	MC 0.063W 0603 1% 6K49	Resistor	1
<b>R10, R12</b>	220R	MC 0.063W 0603 1% 220R	Resistor	2
<b>R11</b>	27R	MC 0.063W 0603 1% 27R	Resistor	1
<b>R13</b>	10k	MC 0.063W 0603 1% 10K	Resistor	1
<b>U1</b>		KSZ8041NL	10/100BASE Physical Layer	1
<b>V1, V2</b>		USBLC6-2P6	TSV-Diode for USB 2.0	2
<b>X3</b>		RJLBC-060TC1	RJ45-Connector with LEDs	1

Table 5-1: Bill of material of the ETH sample schematic

### 5.3.2 Connecting a USB 2.0 Chip

The following example shows how to connect a USB 2.0 chip to the TCM-BF518 Core Module.

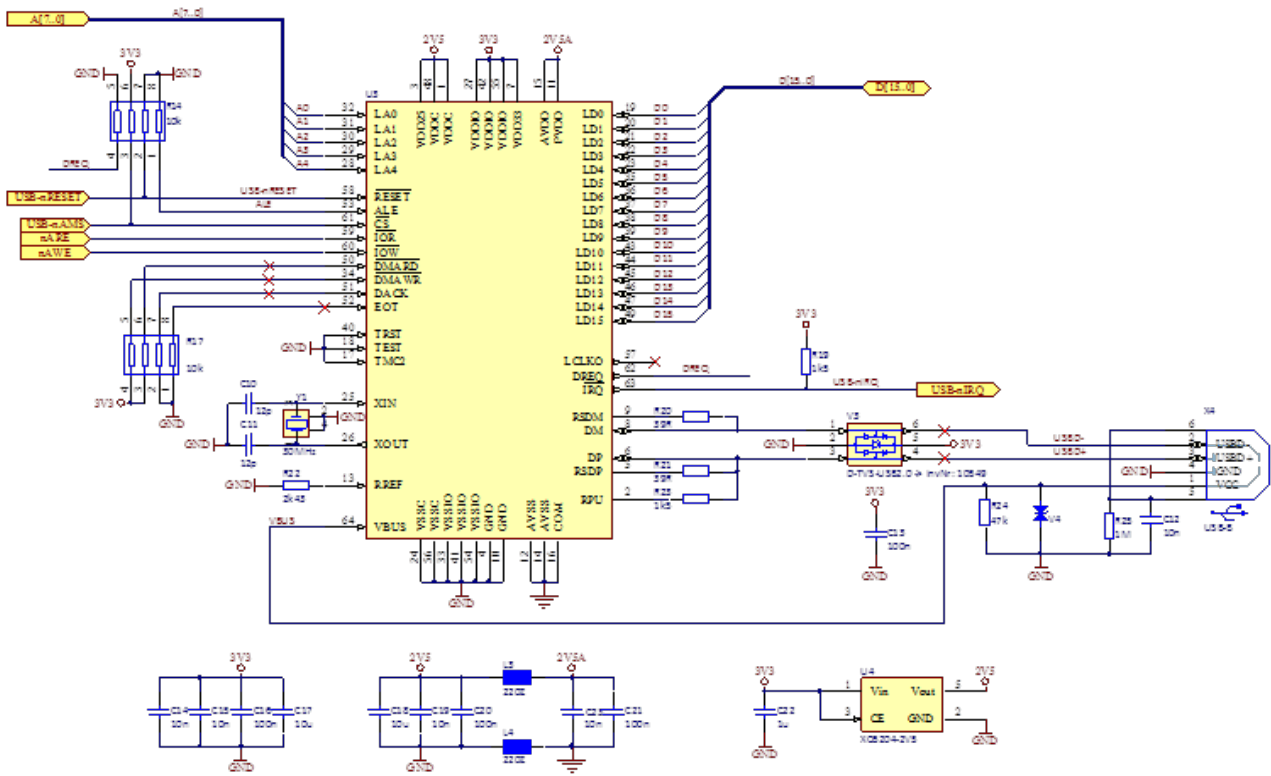


Figure 5-3: Connection of the USB 2.0 chip with the Core Module

Designator	Value	Part Number	Description	Quantity
<b>C1u, C2u</b>	12p	2238 867 15129	Capacitor polarized	non- 2
<b>C3u, C4u, C5u, C9u, C11u</b>	10n	2238 916 15636	Capacitor polarized	non- 5
<b>C6u, C10u, C12u</b>	100n	2238 246 19876	Capacitor polarized	non- 3
<b>C7u, C8u</b>	10u	C0805C106K9PAC	Capacitor polarized	non- 2
<b>L1u, L2u</b>	220R	74279263	Ferrite	2
<b>R1u, R3u, R11u, R12u</b>	10k	MC 0.063W 0603 1% 10K	Resistor	4
<b>R2u</b>	10k	2350 025 11003	4-Resistor Array	1
<b>R4u</b>	1k	MC 0.063W 0603 1% 1k	Resistor	1
<b>R5u, R6u</b>	39R	MC 0.0654W 0603 1% 39R	Resistor	2
<b>R7u</b>	2k43	MULTICOMP	Resistor	1
<b>R8u</b>	1k5	MC 0.063W 0603 1% 1K5	Resistor	1
<b>R9u</b>	47k	MC 0.063W 0603 1% 47k	Resistor	1
<b>R10u</b>	1M	MC 0.063W 0603 1% 1M	Resistor	1
<b>U1u</b>		NET2272REV1A-LF	USB 2.0 Peripheral Controller TQPF	1
<b>V1u</b>		CDS3C05GTA		1
<b>X1u</b>		2411 01	USB-Device Normal	1
<b>Y1u</b>		Q 30.0-JXS32-12- 10/20	Crystal Oscillator	1

Table 5-2: Bill of material of USB2.0 sample schematic

## 6 Mechanical Outline

### 6.1 Top View

Figure 6-1 shows the top view of the Core Module. All dimensions are given in millimeters!

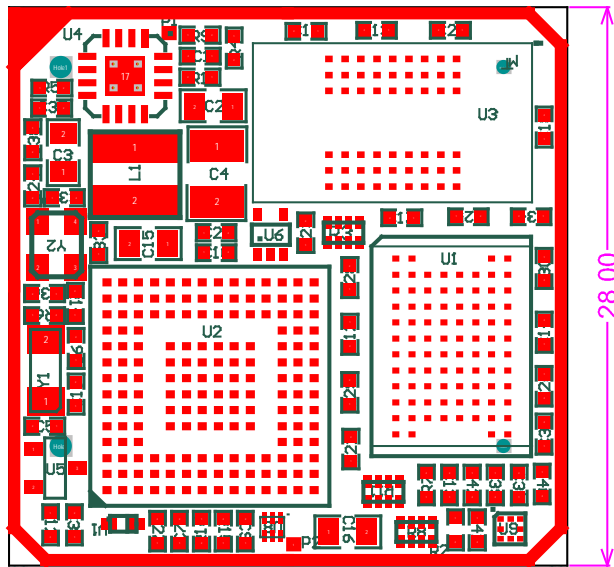


Figure 6-1: Mechanical Outline (**top view**)

### 6.2 Bottom View

Figure 6-2 shows the bottom view of the Core Module (connector version).

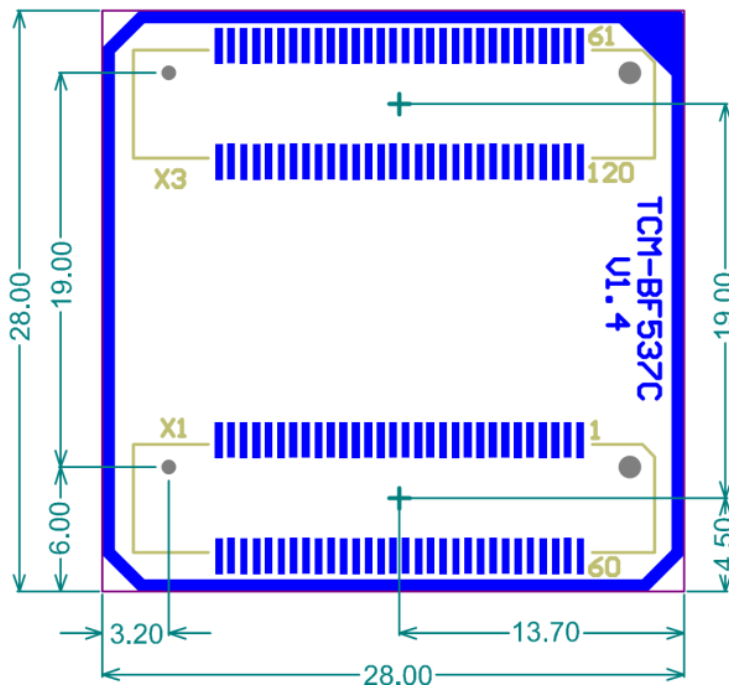


Figure 6-2: Mechanical Outline (**bottom view**)

### 6.3 Side View

Figure 6-3 shows a side view of the Core Module with mounted connectors.

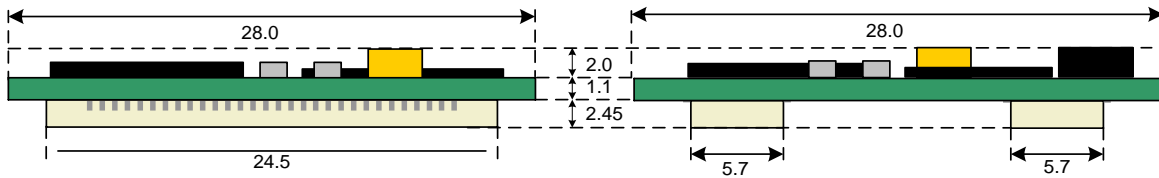


Figure 6-3: Side view with mounted connectors

The total minimum mounting height including receptacle at the baseboard is 5.8mm.

### 6.4 Footprint

The baseboard's footprint for the Connector version (2x Hirose 0.6mm pitch) is shown in Figure 6-4.

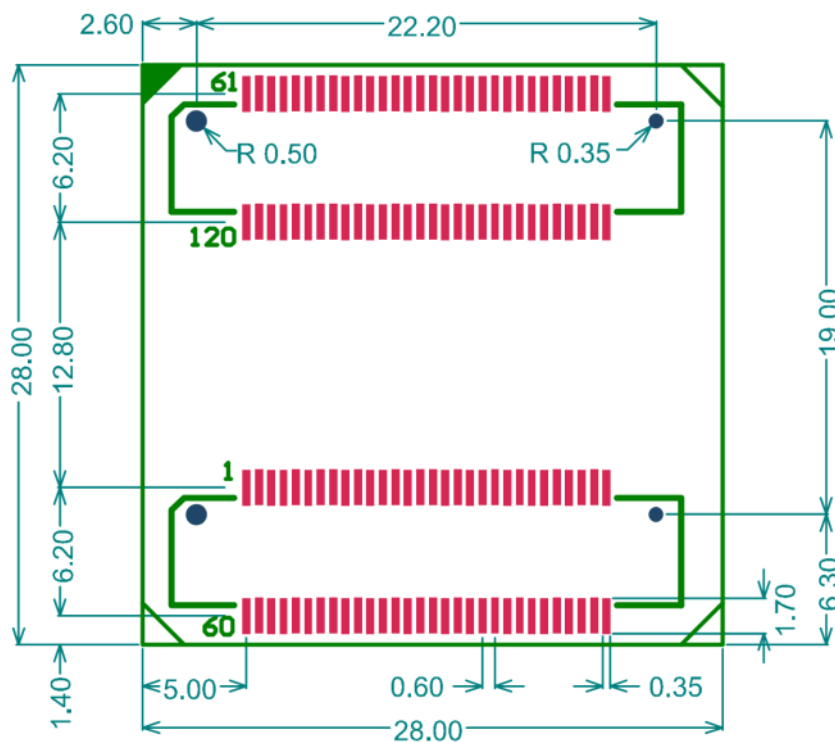


Figure 6-4: Recommended footprint for the baseboard (**top view**)

### 6.5 Connectors

Connector Core Module	Connector (Matching)	Manufacturer	Manufacturer Part No.
X1	X2	Hirose	FX8-60S-SV
X2	X1	Hirose	FX8-60P-SV

Table 6-1: Core Module connector types

The Core Module features 2 connectors. The base board uses the same connectors but oriented in the opposite way.

## 7 Support

### 7.1 General Support

General support for products can be found at Bluetechnix' support site <https://support.bluetechnix.at/wiki>

### 7.2 Board Support Packages

Board support packages and software downloads are for registered customers only <https://support.bluetechnix.at/software/>

### 7.3 Blackfin® Software Support

#### 7.3.1 BLACKSheep® OS

BLACKSheep® OS stands for a powerfully and multithreaded real-time operating system (RTOS) originally designed for digital signal processing application development on Analog Devices Blackfin® embedded processors. This high-performance OS is based on the reliable and stable real-time VDK kernel from Analog Devices that comes with VDSP++ IDE. Of course BLACKSheep® OS is fully supported by all Bluetechnix Core-Modules and development hardware.

#### 7.3.2 LabVIEW

You can get LabVIEW embedded support for Bluetechnix Core Modules by Schmid-Engineering AG <http://www.schmid-engineering.ch>.

#### 7.3.3 uClinux

You can get uClinux support (boot loader and uClinux) for Bluetechnix Core Modules at <http://blackfin.uClinux.org>.

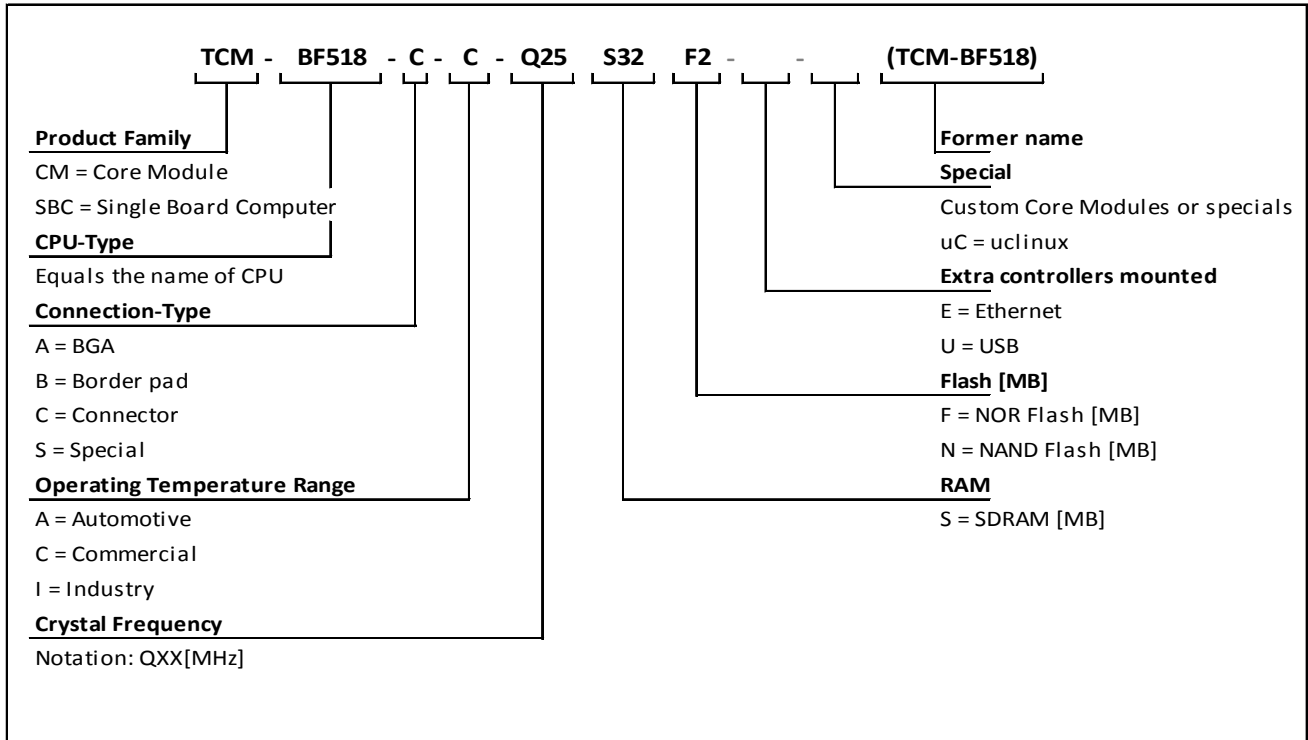
### 7.4 Blackfin® Design Services

Based on more than seven years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

#### 7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of Bluetechnix at <http://www.bluetechnix.com>.

## 8 Ordering Information



### 8.1 Predefined mounting options for TCM-BF518

Article Number	Name	Temperature Range/Description
100-1261-1	TCM-BF518-C-C-Q25S32F2 (TCM-BF518)	Commercial
100-2305-5	EVAL-BF5xx	Blackfin Evaluation Board including accessories
100-2273-1	EXT-BF518-ETH	Ethernet Extender Board for TCM-BF518

Table 8-1: Ordering information

**NOTE:** Custom Core Modules are available on request! Please contact Bluetechnix ([office@bluetechnix.com](mailto:office@bluetechnix.com)) if you are interested in custom Core Modules.

## 9 Dependability

### 9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the Core Module using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all Core Module components except the Blackfin® processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (<http://www.aldservice.com/>) and use the reliability prediction MIL-217F2 Part Stress standard. Please get in touch with Bluetechnix ([office@bluetechnix.com](mailto:office@bluetechnix.com)) if you are interested in the MTBF result.

## 10 Product History

### 10.1 Version Information

#### 10.1.1 TCM-BF518-C-C-Q25S32F2 (TCM-BF518)

Version	Component	Type
1.0.1	Processor	ADSP-BF518KBCZ-4X 0.1
	RAM	MT48LC16M16A2BG-75 IT:D
	Flash	PF48F2000P0ZBQ0

Table 10-1: Overview eCM-BF561-C-C-Q25S128F32 product changes

### 10.2 Anomalies

Version	Date	Description
V1.0	2012 02 06	No anomalies reported yet.

Table 10-2: Overview product anomalies

## 11 Document Revision History

Version	Date	Document Revision
4	2012 02 06	Updated to new design. Removed Boot Mode 3.
3	2010 06 28	Figure 3.5 updated
2	2010 01 26	Layout
1	2009 12 03	First release V1.0 of the Document

Table 11-1: Revision history

## 12 List of Abbreviations

Abbreviation	Description
<b>ADI</b>	Analog Devices Inc.
<b>AI</b>	Analog Input
<b>AMS</b>	Asynchronous Memory Select
<b>AO</b>	Analog Output
<b>CM</b>	Core Module
<b>DC</b>	Direct Current
<b>DSP</b>	Digital Signal Processor
<b>eCM</b>	Enhanced Core Module
<b>EBI</b>	External Bus Interface
<b>ESD</b>	Electrostatic Discharge
<b>GPIO</b>	General Purpose Input Output
<b>I</b>	Input
<b>I<sup>2</sup>C</b>	Inter-Integrated Circuit
<b>I/O</b>	Input/Output
<b>ISM</b>	Image Sensor Module
<b>LDO</b>	Low Drop-Out regulator
<b>MTBF</b>	Mean Time Between Failure
<b>NC</b>	Not Connected
<b>NFC</b>	NAND Flash Controller
<b>O</b>	Output
<b>OS</b>	Operating System
<b>PPI</b>	Parallel Peripheral Interface
<b>PWR</b>	Power
<b>RTOS</b>	Real-Time Operating System
<b>SADA</b>	Stand Alone Debug Agent
<b>SD</b>	Secure Digital
<b>SoC</b>	System on Chip
<b>SPI</b>	Serial Peripheral Interface
<b>SPM</b>	Speech Processing Module
<b>SPORT</b>	Serial Port
<b>TFT</b>	Thin-Film Transistor
<b>TISM</b>	Tiny Image Sensor Module
<b>TSC</b>	Touch Screen Controller
<b>UART</b>	Universal Asynchronous Receiver Transmitter
<b>USB</b>	Universal Serial Bus
<b>USBOTG</b>	USB On The Go
<b>ZIF</b>	Zero Insertion Force

Table 12-1: List of abbreviations

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